MOST SIGNIFICANT BITS

Cyrix to Enter PC Business

Crossing a line that even Intel fears to tread, Cyrix will sell complete PC systems based on its 6x86 processor. The move, however, is not as outlandish as it first appears. The company plans to focus entirely on "hot box" system configurations with the fastest available memory, disks, and graphics. Presumably, these high-end systems will carry a large price tag, leaving the mainstream price points to Cyrix's chip customers. The company also plans to sell only tens of thousands of systems this year, further avoiding direct competition between Cyrix and other makers of 6x86 PCs.

So what's the point? This strategy has two primary benefits for Cyrix. First, it ensures a high-performance commercial platform is available to generate optimum benchmarking results. Instead of using an in-house "development system," Cyrix can benchmark on a system that anyone can buy. In contrast, IBM was unable to publish best-case benchmarks for the PowerPC 604 when it was first released because only midrange configurations were available for sale.

The second benefit is in creating a premium brand image for Cyrix and its 6x86 product. To date, PC buyers know Cyrix (if at all) for providing low-cost alternatives to Intel products. Its chip customers use a similar business model and do little marketing. The system campaign allows Cyrix to reposition itself by advertising the performance benefits of its 6x86 systems and allowing a head-to-head comparison with Pentium PCs. Even if readers don't buy the Cyrix system, the company hopes its new high-performance image will convince them to buy 6x86 systems from other PC makers.

To minimize the financial impact on Cyrix, the company is relying heavily on third parties to build and support the Cyrix-brand PCs. The company has selected Electronic Data Systems (EDS) to assemble the systems from externally fabricated motherboards and other components. Cyrix itself will bear little inventory and other direct costs. The company does not expect PC sales to be a significant portion of its overall revenue in the near term.

The decision to sell systems is a bold and untraditional move. Cyrix says it has discussed the plan with its major customers with little dissent, for good reason. These vendors will lose few, if any, sales to Cyrix, and the Cyrix hot box should act as a flagship, leading the entire fleet of 6x86 systems to new victories.

IBM Updates POWER Plans

While Somerset cranks out the mainstream PowerPC chips, IBM continues to develop its own chips for in-house use. The company's RS/6000 workstation line alone rakes in $7 billion per year, and the AS/400 minicomputer line is also now running on PowerPC, so there is adequate revenue to fund this development.

The AS/400 currently relies on PowerPC processors called the A10 and A30 *(see* **091004.PDF***)*. IBM's Rochester (Minn.) division is developing Apache, a follow-on to the A10 that is due in systems in mid-1997. The new chip will move the A10 design to IBM's 0.35-micron CMOS-5X process, allowing larger caches and pushing clock speeds to 150 MHz or above. It also includes multiprocessing capability. We estimate this design will deliver performance similar to the 604e on SPECint-type benchmarks.

Although Apache is intended primarily for the AS/400 line, the 64-bit device may be used in some RS/6000 systems instead of the star-crossed PowerPC 620. The 620, Somerset's first 64-bit chip, is now slated to ship in 2H96, a year later than originally planned; if it slips much further, Apache will be available to add 64-bit capability to the RS/6000.

The RS/6000 line currently relies on the Power2 processor, now running at up to 77 MHz, at the high end. IBM is developing a single-chip device dubbed Power2 SuperChip (P2SC). Like the Power2, P2SC is a 32-bit implementation. It combines the core functions of the Power2 chip set, with reduced caches, into a single chip. The P2SC is due in systems late this year. The chip's integer performance may be similar to the 604e's, but the P2SC will shine on floating-point and transaction-processing benchmarks.

The P2SC will be succeeded by the PowerPC 630 in 2H97. This single-chip device is designed for maximum performance where cost is no object. As with the P2SC, floating-point speed and memory bandwidth are key areas of focus.

To date, Somerset's PowerPC designs have been driven by Apple's criteria: strong integer performance at a low cost. Many of IBM's customers, in contrast, are high-end scientific and commercial users, leaving Big Blue to develop its own processors to meet these needs. These processors may be offered to other companies, but with a small market for these expensive workstation engines, it seems unlikely they will see the light of day outside of IBM.

PA-8000 Schedule Slips

While less troubled than the PowerPC 620, HP's PA-8000 processor has also hit a snag. The company announced it is currently shipping limited quantities of PA-8000 systems to key software developers, but no formal system announcements are in sight. The PA-RISC vendor had previously indicated the PA-8000 would ship in 1Q96.

We believe HP is having problems fabricating the enormous (345-mm^2) die with significant yield, a problem also encountered by the R10000. It may take a quarter or so to improve yields enough for volume system shipments. This delay puts the PA-8000 squarely in the crosshairs of Digital's 400-MHz 21164, slated to deliver 11 SPECint95 and 15 SPECfp95 in 2Q96. Thus, the slip will make it more difficult for HP to leap into the performance lead, as it had expected.

AMD Axes NexGen 586

As we predicted *(see* **091701.PDF***)*, AMD's shipment of the 5K86 on schedule *(see* **100401.PDF***)* led to a decision to discontinue the Nx586. Although the latter processor offers better performance than the 5K86, the NexGen device used a nonstandard bus and pinout, making it incompatible with common PC motherboards. Before its merger with AMD, NexGen had managed to sell a few hundred thousand Nx586 chips, but once the merger was announced, sales trailed off dramatically.

AMD will continue to supply existing Nx586 customers from inventory but will obtain no new chips from its foundry, IBM. The company can now focus its marketing efforts on the 5K86 while its engineers work on its follow-on, the K6. By discarding the Nx586, AMD makes it clear that the returns on its $615 million investment in NexGen will not accrue until the K6 begins shipping next year.

SMC Buys Efar, Enters Chip-Set Business

Standard Microsystems Corp. (Hauppauge, N.Y.) has acquired chip-set maker Efar Microsystems for $5.6 million, jumping into the competitive PC chip-set market. SMC's semiconductor business—about $150 million in its fiscal 1996—has been based largely on PC I/O chips, including LAN controllers, disk controllers, super I/O chips, and an "Ultra I/O" chip that also integrates the keyboard controller and real-time clock. Recognizing that, in time, these functions will be merged with core-logic chips, SMC acquired Efar to gain access to core-logic designs and employees with expertise in that area.

Efar is a four-year-old 14-employee company based in Santa Clara (Calif.), with a branch in Taiwan. The company has sold 1.2 million chip sets over the past four years, primarily to Asian motherboard and computer makers, including Acer, Mitac, and DFI; Alaris, Cache, and Amptron are its top U.S. customers.

SMC owns a fab in New York, but it runs an ancient 2-micron process used for ink-jet print heads, pressure sensors, and RC networks. For its VLSI products, SMC is essentially a fabless company. To obtain guaranteed capacity for its I/O chips, the company made a $12 million investment in AT&T's Madrid fab and a $20 million investment in Chartered Semiconductor (Singapore). The core-logic products initially will be built by TSMC (Taiwan).

The company disclosed plans for two new Pentium/PCI chip sets that will ship later this year. The UltraCore chip set has a partitioning similar to Intel's Triton design and, the company claims, comparable performance. More interesting is the UltraCache design, which integrates a 256K cache memory into the bridge chip to reduce system cost.

Efar developed the cache-memory design in partnership with MoSys; the cache is based on the MoSys multibank DRAM structure, allowing it to achieve 3-1-1-1 performance (comparable to synchronous burst SRAMs) at 66 MHz using a low-cost design with only one transistor per bit. Price and availability for the chip sets have not been disclosed; production is planned for later this year.

Because of its strong role in the PC I/O business, which it shares primarily with National, SMC has a foot in the door at nearly every PC maker worldwide. The company hopes to leverage this sales presence to boost the market for Efar's chip sets. In the long run, SMC will integrate its I/O chips with the core logic; its goal is to produce an "everything else" chip to complement the microprocessor and memory. Successful completion of this strategy will require graphics and multimedia expertise; an acquisition in this area is likely to be next.

LSI Samples Chip Set for Set-Top Box

LSI Logic has made good on its promise to leverage its MIPS cores and ASIC experience to create an economical television set-top box. The chip set, the Integra 1000, is based on LSI's tiny CW4001 MIPS processor core *(see* **081703.PDF***)* and a number of the company's existing MPEG-2 decompression cells. The three-chip set will begin limited sampling in April, with general sampling several months later. In high volume, the product is priced at about $75.

The Integra 1000 consists of three chips: the L64008 controller, the L64005 MPEG-2 decoder, and either the L64704 (for satellite systems) or the L64768 (for cable systems) receiver. Both the 64008 controller and the 64005 decoder connect directly to DRAM for their local memory. LSI expects a typical set-top box to contain 512K of DRAM for the CPU plus another 2M for the decoder.

The controller's MIPS core, running at 54 MHz, includes a unified 1K cache, several serial interfaces, and timers. The total die size of the 0.5-micron device was not revealed, but the CW4001 core and cache account for approximately 20% of the area of the L64008.

The chip set decodes and decompresses the I, P, and B frames of MPEG-2 data streams in either 720 × 480 × 30 frames/s (NTSC) or 720 × 576 × 25 frames/s (PAL) format. Audio decoding and an on-screen graphics overlay are also supported. The three chips communicate over a shared bus and via dedicated chip-to-chip interfaces. With the addition of DRAM, audio and video DACs, and other components, LSI estimates the bill of materials for a typical set-top box will cost less than $200 in volume.

Although the market prospects for TV set-top decoders are still uncertain, LSI is attempting to jumpstart the market with the Integra chip set. The company has not named any customers for Integra, although some certainly must exist. The 64008 will now compete with IBM's 403Gx, the ARM 7500, and NEC's R4300, among others, for the distinction of becoming the first set-top processor to reach volume.

Erratum: S3 ViRGE

In our recent article on 3D accelerators *(see* **100304.PDF***)*, we misspelled the name of S3's product. The correct name is ViRGE: Video and Rendering Graphics Engine. M

