PATENT WATCH

by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send comments or questions via e-mail to belgard@umunhum.stanford.edu.

5,469,561

Apparatus and method for controlling the running of a data-processing apparatus
Issued: November 21, 1995
Inventor: Koji Takeda
Assignee: Seiko Epson
Filed: December 22, 1992
Claims: 24
A clock signal supplied to the CPU is varied based on the bus cycle or address of a device, such as memory or an I/O device, which is identified by the CPU for processing data. Alternatively, the frequency of the clock signal is varied based on ambient temperature and line-voltage conditions. Therefore, speed of the CPU can be varied to accommodate high - speed memory devices and slower-speed I/O devices.

5,469,551

Method and apparatus for eliminating branches using conditional move instructions
Issued: November 21, 1995
Inventors: Richard L. Sites, et al
Assignee: Digital
Filed: May 31, 1994
Claims: 21
In a RISC processor, by providing a conditional move instruction, many short branches can be eliminated altogether. A conditional move instruction tests a register and moves a second register to a third if the condition is met; this function can be substituted for short branches and thus maintain the sequentiality of the instruction stream.

5,469,544

Central processing unit address pipelining
Issued: November 21, 1995
Inventors: Deepak J. Aatresh, et al
Assignee: Intel
Filed: November 9, 1992
Claims: 20
A microprocessor that pipelines addresses for both burst and nonburst data transfers. By pipelining addresses, the microprocessor is able to increase the throughput of data transfers in the system. Bits are used that may be programmed to disable and enable the address pipelining for the nonburst and burst transfers. This patent appears to apply to the P6 (Pentium Pro) bus.

5,467,476

Superscalar processor having bypass circuit for directly transferring result of instruction execution between pipelines without being written to register file
Issued: November 21, 1995
Inventor: Takashi Kawasaki
Assignee: Toshiba
Filed: August 19, 1994
Claims: 4
A superscalar parallel processor, having a plurality of pipelines arranged to execute a maximum of N (N > 1) instructions in parallel, includes a bypass circuit for transferring a data output of each stage of at least two pipelines between the pipelines.

5,467,473

Out-of-order instruction load and store comparison
Issued: November 14, 1995
Inventors: James Kahle, et al
Assignee: IBM
Filed: January 8, 1993
Claims: 19
A processing system allows for out-of-order instruction execution and includes at least one load/store unit for loading instructions to a register for processing by a fixed-point unit, floating-point unit, or the like, and store the results to memory. A load queue maintains the addresses and program numbers of the load instructions. During execution, the address of the store instruction is compared to the address in the load queue of previously executed load instructions.

5,440,749

High-performance low-cost microprocessor architecture
Issued: August 8, 1995
Inventors: Charles Moore, et al
Assignee: Nanotronics (now: Patriot Scientific)
Filed: August 3, 1989
Claims: 29
A microprocessor includes a CPU and a separate DMA processor. The main CPU is a simple, nonpipelined stack machine, and therefore executes a simple stack instruction set quickly. The DMA CPU allows instructions to execute four times faster than the RAM speed by fetching four instructions in a single memory cycle. This invention is claimed to be embodied in the ShBoom microprocessor being touted as a Java processor. M