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THE INSIDERS' GUIDE TO MICROPROCESSOR HARDWARE

Intel, Cyrix Reach P200 Level

Pentium Ships First But 6x86 Has Slight Performance Edge

by Linley Gwennap

Underscoring the tight performance race between the two vendors, Intel and Cyrix extended the performance of their mainstream processors to the P200 level at nearly the same time. Intel's 200-MHz Pentium processor is available in volume immediately, offering a 7–9% performance boost over the Pentium-166, as Figure 1 shows. Cyrix's 150-MHz 6x86, which the company sells as the 6x86-P200+, will ship in limited quantities later this month, with volume production slated for August. Testing at MDR Labs revealed the Cyrix chip outperforms the newest Pentium by 3–5% on Ziff-Davis's Winstone 96 and Winstone 32 benchmarks.

Intel, of course, has been shipping 200-MHz Pentium Pro processors for several months, but given PPro's problems with 16-bit code, the new chips outperform PPro on the Winstone 96 benchmark, which includes popular 16-bit applications running under Windows 95. Although PPro is still the fastest processor on 32-bit applications, the Cyrix 6x86 delivers the most performance within the popular P54C pinout, giving PC makers an easy upgrade for their current systems.

Intel Takes P54C to the Limit

The 200-MHz speed grade represents the end of the line for the two-year-old P54C design, which recently surpassed Intel's 486DX2 as the best-selling PC processor of all time. Starting with the original 0.5-micron BiCMOS versions at 90 and 100 MHz, the company pushed the clock speed higher and higher over time through circuit tuning and a shrink to 0.35-micron BiCMOS, producing a version known as P54CS.

Getting the part to yield at 200 MHz was no small task. While a CMOS design will yield a small number of parts well above the center point of the clock-speed curve, BiCMOS parts have a narrower yield curve. Most of Intel's parts have been yielding at 150 to 166 MHz.

To reach 200 MHz, Intel has taken several steps. First, a combination of a few circuit changes to speed critical paths with some process improvements to reduce the effective gate length moved the speed curve slightly higher. To further improve the operating frequency, Intel revived the VRE voltage specification for the Pentium-200, which requires a 3.45-V supply. This specification was used to improve the yield of early Pentium-100 chips. Increasing the voltage by 5% provides a similar improvement in clock speed.

A new plastic PGA package also helps the clock frequency. Instead of using the traditional ceramic substrate, the PPGA mounts the die on a standard PCB. The heat sink attaches to a heat slug mounted directly on the die, providing better thermal characteristics than a typical CPGA package, which has a layer of ceramic between the heat sink and die. With this arrangement, the die can operate at a higher temperature and thus tolerate a higher clock speed. Because it uses copper traces on FR4 rather than tungsten through ceramic, the PPGA has better electrical characteristics as well. Thus, the chip can run slightly faster. We believe the new package also reduces Intel's manufacturing costs.

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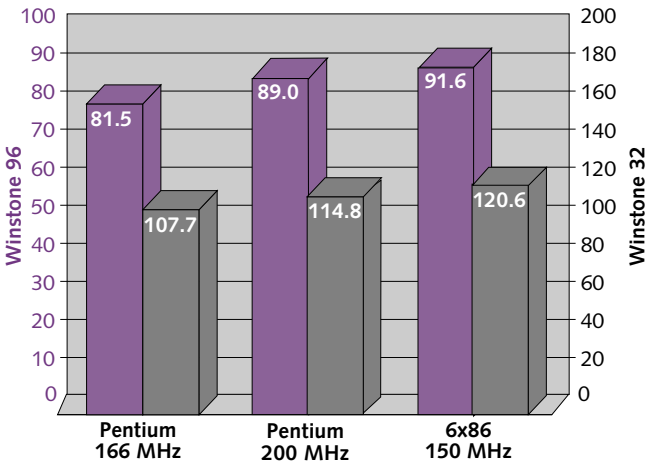

Figure 1. On two PC benchmarks, the new 200-MHz Pentium outscores the Pentium-166 by 7–9%. Cyrix's new 150-MHz chip, dubbed the 6x86-P200+, is 3–5% faster than the Pentium-200. See article text for configurations. (Source: MDR Labs)

AT A GLANCE

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THE PUBLISHER'S VIEW

Intel's Competitors Stuck in Third Tier

Taking On Intel's Design and Manufacturing Is Only the Start

Ever since the debut of the IBM PC 15 years ago, Intel has been the dominant force in microprocessors for personal computers. During this time, competitors have tried a variety of strategies to capture some of Intel's market share, with limited success. Today, Intel's position appears stronger than ever, and its challengers—whether x86 or RISC—are increasingly being forced to seek customers among third-tier PC makers to survive.

The challenges in competing with Intel are many. Intel's vast capital resources, the fruit of many years of highly profitable, high-volume microprocessor sales, have given the company a big lead both in the size and number of its design teams and the scale and sophistication of its manufacturing capability. Even if the formidable design and manufacturing hurdles can be overcome, however, Intel's competitors face another challenge: Intel's dominant position has given the company enormous clout that it can—and apparently does—use to engender grave doubts in the mind of any PC executive flirting with the idea of using competitive chips.

Consider the difficulty Cyrix and IBM have getting design wins for the 6x86. This chip delivers better performance than the fastest Pentiums on typical Windows applications, giving Cyrix—along with its foundry and marketing partners, IBM and SGS-Thomson—a strong product offering (see page 1). Yet Acer is Cyrix's only design win among leading PC makers.

There are some technical reasons that have contributed to Cyrix's difficulty in signing up big-name customers. The 6x86 is power-hungry, requiring substantially more cooling than Intel's Pentium, and its performance on floating-point code falls short. But the biggest challenge Cyrix and its partners face is Intel's clout with its customers—and the fear these customers have about how Intel may respond.

We have heard no first-hand accounts of Intel's conversations with its large customers. But sources at several of Intel's competitors describe a consistent pattern. When a PC maker shows serious interest in a non-Intel processor, the competitors say, a visit from Intel's top executives soon follows. They explain that using a non-Intel processor could affect the relationship between Intel and the PC maker, perhaps making Intel more cautious about revealing future product roadmaps or providing early silicon samples. The message that many PC makers seem to get—although it is presumably never stated—is the availability of leading-edge Intel processors might also be affected.

Intel is well aware, of course, of its dominant position and the obligations that accompany this position if the company is to stay clear of antitrust-law violations. Intel surely has top-notch legal advice and would not carelessly endanger its position with strong-arm tactics. But the irony is there is no need for Intel to use such tactics—so many people in the industry assume that Intel would find ways to retaliate against companies using competitive processors that no threats are necessary.

Given the widely held fear that using a competitive processor could impact a PC maker's ability to get leading-edge processors from Intel, the competitors' lack of a full product line limits the prospects for the chips they do have. Cyrix—and some day AMD—might offer a good desktop solution, but what about the portable line, where power consumption is key? What about servers, where Pentium Pro with its multiprocessor-ready bus is needed? No competitor can match Intel's product spectrum today. It is possible that AMD will have a good notebook processor in 1997, but it is unlikely that it will have chips with multiprocessor capabilities matching Intel's P6 family.

The view PC makers take of the alternatives varies, but they can be divided into three broad categories. The Intel Loyalists, such as Dell, Gateway, and Packard-Bell, are unlikely to seriously consider alternative processors anytime soon. The best long-term prospects for Intel's competitors are the Big Independents—companies such as Compaq, Acer, AST, and even HP, which are confident enough to risk Intel's ire and want to reduce Intel's influence over their product directions. These companies also seek to use their R&D efforts to differentiate their products from those of the Intel Loyalists; one approach is to use some non-Intel processors. So far, these companies have used non-Intel processors mostly in low-end products, but once high-speed 6x86 chips are available in high volume, this could change. Compaq has retreated from alternative processors for now, but this change appears to have been driven more by the lack of volume availability than by any newfound love for Intel.

In the meantime, most of the volume for Intel's competitors will come from the Countless Unknowns—the great masses of PC makers whose names are largely unknown but which collectively ship a significant fraction of the industry's computers. While unglamorous, this market is big enough for the alternative processor makers to succeed on a modest scale while they continue preparing for future assaults on the top tier. M

Sun Signs Four Java Chip Makers

Sun Microelectronics has announced the first four intended licensees for Java microprocessors. LG Semicon, Mitsubishi, NEC, and Samsung are expected to begin manufacturing Java chips for both commercial use and internal consumption in 1997.

None of the four companies is yet a licensee; each has signed a "memorandum of understanding" avowing interest in the Java chips, but the details of each license agreement are still being negotiated. Assuming all goes well, each vendor will receive from Sun a design package including RTL models, simulation tools, test vectors, and other deliverables.

All four potential licensees have several characteristics in common: large manufacturing capacity, a brand name in consumer electronics, a major market presence and distribution channel, and commitments to use Java chips for internal consumption. This strategy was deliberate, and Sun expects to increase the ranks of Java-chip manufacturers within a few months, adding vendors from the U.S., Europe, Taiwan, and Japan. We believe Philips, Motorola, Toshiba, and Hitachi may be among the second-round candidates.

Part of the licensee selection criteria involved commitments for substantial internal consumption. None of the four companies has said publicly what they intend to do with their Java chips, apart from some musings regarding cellular telephones, intelligent home appliances, and network computers.

Currently, Sun is licensing only the PicoJava core, not the peripheral logic or bus interface used on MicroJava (see MPR 2/12/96, p. 4). Each licensee will develop its own application-specific implementations, possibly competing head-on with Sun's own versions of MicroJava. At this stage, Sun is more interested in seeding the market with Java processors (and collecting royalties therefrom) than in dominating the market with its own implementations.

Each of the licensees already has at least one embedded microprocessor line, although each emphasized that the Java core was not intended to replace any current product line. Mitsubishi, for one, recently launched its new embedded CPU/DRAM family with the M32R/D (see MPR 5/27/96, p. 10). Since all four vendors are major memory producers, future chips that merge a PicoJava core with substantial amounts of on-chip DRAM might not be far off.

Separately, Sun announced the first customer for Java chips: Northern Telecom. The telecommunications giant plans to embed Java processors in future telephones for home and business use. These telephones would be able to access the Internet in addition to their standard functions, so the Java chips would be useful in executing downloaded content. The Java phones are expected to begin appearing next year. Given the interest level of four major chip makers, more customers must be in the pipeline.

AMD Boosts K5 to 100 MHz

As both Intel and Cyrix announced parts with Pentium-200 performance (see cover story), AMD has just reached the 100-MHz level with its K5 processor. The company reaches this milestone a bit ahead of schedule; when it announced its 90-MHz K5 (see MPR 3/25/96, p. 1), AMD expected volume shipments of the 100-MHz version in 3Q96.

The company has changed its nomenclature for the device. Originally code-named the K5, the part was first announced as the 5K86. Now the company has backtracked, using K5 as the official product name. AMD continues to compare its parts to Intel's using the P-rating system, but it now uses the suffix PR instead of merely P. (Cyrix continues to use the P suffix.) Thus, AMD's new chip is known as the K5-PR100, with performance similar to that of a 100-MHz Pentium processor.

The PR100, now shipping in volume, is priced at $84 in quantities of 1,000, a whopping 37% below Intel's list price for the Pentium-100. AMD is committed to delivering its K5 chips for at least 25% less than Intel's prices. The company has cut the price of its K5-PR90 to $67 and the K5-PR75 to $55. These prices mirror the relatively small gaps between Intel's Pentium pricing at 75, 90, and 100 MHz.

Moving to the Pentium-100 level ahead of schedule helps AMD, but the gain is not enough to propel it above the $100 price point. In fact, the price of AMD's best K5 chips has dropped from $99 to $84 in less than three months, despite the clock-speed boost. At these prices, profitability for AMD's chips is poor, and the company is restricted to the lowest-price portion of the market, preventing it from gaining significant share.

The next step for the K5 is a new version that AMD expects to boost per-clock performance by 20%. The company plans to ship this enhanced K5 by September. With Intel moving the low-end market to the Pentium-120 by the end of the year, AMD needs this version to keep pace and perhaps even get prices into three digits again.

First PA-8000 Workstations Appear

After a three-year hiatus, HP is again shipping the industry's fastest workstations. The HP9000 Model C180-XP, using a 180-MHz PA-8000 processor with 1M of instruction cache and 1M of data cache, delivers 10.8 SPECint95 and 17.2 SPECfp95 (base), surpassing the fastest Alpha workstations from Digital. The HP system has an entry price of $49,850 in a configuration with 32M of memory, a 2G disk, and a 17" color monitor. The company also offers a 160-MHz system, appropriately called the Model C160, that has an entry price of $22,520.

These systems are the first workstations from HP to include PCI expansion slots. HP sells PCI-based personal computers and can now use the same PCI cards in both

product lines. IBM and Digital, which both also have PC and workstation lines, also offer RISC workstations with PCI slots. The HP workstations do not, however, take advantage of any PCI-based devices on the motherboard. In the future, HP may be able to lower its build costs by using standard PC chips for basic I/O and networking functions.

The company also formally announced K-class servers using the PA-8000, which it has been shipping since April (see MPR 4/15/96, p. 4). The HP9000 K260 and K460 support up to four 180-MHz processors and come standard with 128M of memory. Prices start at $62,245. Because these systems are designed with many banks of memory, SPECfp95 performance is slightly better than on the C180; the K460, with 32-way interleaved memory, rates at 18.3 SPECfp95 (base). The SPECint95 score, which mainly focuses on CPU-cache interaction, is unaffected by this change to main memory.

The photo at right shows the PA-8000 chip mounted to a daughterboard with dual external 1M caches. To support the two 128-bit data paths to the caches plus tag bits, control signals, and the 64-bit system bus, more than 1,000 connections are required between the die and board. Many of these connections carry power; the PA-8000 consumes well over 40 W peak. (The company would not provide more precise figures.) Instead of using an extremely expensive PGA package, HP mounts the die to the board using flip-chip attachment, completely eliminating the package.

The new announcements are a huge step forward for HP, raising the SPECint95 performance of its high-end workstations by more than 2.5× in one fell swoop. The company gained prominence in the workstation industry in the early 1990s by grabbing the performance lead with its original PA-RISC systems, but HP lost the workstation performance lead to Digital in 1993. The PA-8000 overcomes the disappointment of the PA-7200 and thrusts HP back into the spotlight. It may be difficult to stay there, however; Digital continues to aggressively push the clock speed of its Alpha chips and is likely to surpass HP's performance soon.

TI Promotes 0.25-Micron Effort

In a widely publicized nonannouncement, Texas Instruments hyped its forthcoming 0.25-micron CMOS process. The company believes this process, which it refers to by its effective gate length of 0.18 microns, will eventually enable chips with as many as 125 million transistors. Even with such an advanced process, such a design would be quite large, 19 × 19 mm, and expensive to build. Furthermore, the only way to reach such high transistor counts would be to devote most of the transistors to memory. Intel, for example, today builds a 30-million-transistor cache chip for the Pentium Pro in 0.35-micron CMOS.

The new process is a future derivative of TI's EPIC-4 process (see MPR 7/10/95, p. 16). The company is currently sampling UltraSparc-2 processors built in a 0.29-micron version of EPIC-4 and expects these parts to reach production in 3Q96. The first products in the 0.25-micron process are scheduled to sample late this year, with volume production in 1H97. The company did not disclose specific product plans, but the first devices are likely to be versions of UltraSparc-2 and TI's multiprocessor MVP DSP. Neither of these chips is likely to approach 125 million transistors.

Of course, many other vendors are also developing quarter-micron processes. If TI can stick to its schedule, it may be one of the first to reach this milestone; Intel, for example, does not expect to ship 0.25-micron parts until 2H97. These advanced fabrication processes will certainly give chip designers a significant increase in transistor count to play with. But don't expect a 100-million-transistor CPU chip in the next few years.

Few Newsletters Misprinted

A few subscribers have noted that their copies of *Microprocessor Report* arrived recently with missing or duplicated pages. We are working with our bindery to solve this problem and do not expect any such errors in the future. If you have received any newsletters with printing errors, please contact our customer service department (see page 2); we will be happy to send you a corrected copy. Thanks for your support.

Sigma Launches MPEG-1 for Video CD

Sigma Designs (Fremont, Calif.), formerly a graphics-board vendor, has recently redirected its business to become a multimedia component supplier. The RealMagic EM8000 is the first product released under this new guise.

The EM8000 is the first chip to integrate MPEG-1 audio and video decoding plus X-Y scaling in a single device. Based on horizontal and vertical bilinear interpolation, the Sigma chip's proprietary video-scaling scheme permits the display of a clear video image in sizes ranging from a postage stamp to a full screen.

This chip is well designed for video CD players. These devices are popular in Asia, where they are used as karaoke machines and movie players, but they have seen little action in other geographical areas. Within one or two years, these systems will be obsoleted by DVD players.

The chip also has a glueless interface to the ISA bus, enabling EM8000 PC add-in cards. These would be most useful in older PCs, as most recent Pentium systems can perform MPEG-1 decoding in software.

Sigma offers a reference design to OEMs with a complete turnkey manufacturing kit. The EM8000 is sampling now, with full production expected in 3Q96. The unit price is $41 in 1,000-piece quantities. This price is a bit expensive, even for the level of integration offered; MPEG-1 video decoders sell for $25 or less, and audio is easily handled by the host CPU. The EM8000 will be more useful in a standalone video system than a PC. M

P200

Continued from page 1

The PPGA package fits into the same socket as the CPGA Pentium and uses similar heat sinks, so board makers should be able to interchange the two parts. One proviso: the board must be designed to deliver the VRE voltage level, which is tolerable to non-VRE Pentiums as well. Intel will offer the 200-MHz Pentium only in the PPGA package; the Pentium-166 will be offered in the PPGA as well as the standard CPGA. Intel is likely to use the new package for other high-speed parts in the future.

The 200-MHz clock speed pushes power dissipation to 15.5 W (maximum) at 3.45 V. The faster clock also improves performance to 5.5 SPECint95 and 2.9 SPECfp95 (base). This integer score is slightly better than that of the 200-MHz 603e (see MPR 5/27/96, p. 13), but the FP score lags the PowerPC chip's.

Bandwidth Problem Looms

Achieving even higher clock speeds from the current Pentium design will not be possible. Intel's next process shrink is to a 0.28-micron process (see MPR 7/10/95, p. 16), but this process eliminates bipolar devices, requiring a pure CMOS design. Intel is working on a new design, the P55C, that utilizes the 0.28-micron CMOS process, but it is not expected to ship until late this year. It isn't clear whether even the P55C will exceed 200 MHz, as the missing bipolar transistors may offset the gain from the gate shrink and the new process makes no improvements to the critical metal layers.

The P55C addresses one key problem with the P54C design: the current chip has run out of bus bandwidth. The 200-MHz Pentium runs at three times the clock speed of the original Pentium yet uses the same 66-MHz bus. This bottleneck has been exacerbated over the past few years by the increased size and complexity of typical application software. As a result, the Pentium-200 scores just 9% better than a Pentium-166 on Winstone 96 despite a 20% faster clock. A 180-MHz Pentium, with just a 60-MHz bus, would do worse than a Pentium-166, which is why Intel skipped that speed grade.

The P55C doubles the size of the on-chip caches, to 16K for instruction and 16K for data, reducing the number of external cache accesses. This change, combined with minor improvements over the P54C pipeline, will give the P55C-200 about 15% better performance than the Pentium-200, according to Intel. The performance improvement at lower clock speeds may be less.

Short Lifespan for Pentium-200

Intel is selling the Pentium-200 for $599 in quantities of 1,000, a 20% premium over the Pentium-166 despite the relatively modest increase in performance. We expect this price to drop to about $450 by the end of the year. Once the P55C is available, the Pentium-200 will disappear fairly quickly, perhaps as soon as mid-1997.

We expect Intel to offer aggressive pricing on the P55C, phasing out the Pentium-200, for two reasons. First, the P55C includes Intel's new MMX multimedia instructions (see MPR 3/5/96, p. 1), which the company wishes to move into the PC mainstream as quickly as possible. Second, we do not believe the speed yields on the P54C design at 200 MHz are adequate to support the volumes required to move that device into the sub-$300 portion of the market. Thus, the Pentium-200 is simply a bridge product filling the gap between the Pentium-166 introduction in January and P55C production late this year.

Cyrix Improves Bandwidth with 75-MHz Bus

Due to its more efficient microarchitecture, Cyrix's new part exceeds the performance of the Pentium-200 while operating at just 150 MHz. To achieve this performance, Cyrix has pushed the bus speed of its part to 75 MHz; Pentium, in contrast, is limited to 66 MHz. This change improves the bandwidth to the rest of the system by 14%, easing the bottleneck seen by the 200-MHz Pentium.

Cranking up the bus speed, however, can make life more difficult for the motherboard designer. Cyrix is working closely with chip-set and motherboard vendors to enable the 75-MHz bus speed. VLSI Technology announced that its Lynx chip set, available today, will support the 75-MHz bus. This chip set operates the PCI bus asynchronously, allowing it to remain at 33 MHz. The faster bus speed, however, requires more expensive cache SRAMs.

Cyrix expects Opti, SiS, and VIA to add 75-MHz system-bus support to their Pentium chip sets in the near future; none of these vendors has committed to this plan. Motherboards supporting the 75-MHz bus are available from Diamond Flower, Inc. (DFI), with First International Computer (FIC) expected to become a second source.

The 150-MHz 6x86 does not support the 2.5× clocking mode found in Pentium, which would have allowed a 60-MHz bus. It does support a 3× clocking mode, but Cyrix is discouraging its use, as this configuration would not match a Pentium-200 in performance. Thus, potential 6x86-P200+ customers are limited to a single chip set and a single motherboard vendor today, with the possibility of a small number of vendors in the future.

The company is investigating pushing the bus speed even further, to 83 MHz. This increase would support a 166-MHz 6x86 that could be deployed in 4Q96, maintaining the 2× ratio. Without the faster bus speed, however, the 166-MHz version would offer no better performance than the 150-MHz part, so there would be little point in offering it. An 83-MHz system bus is challenging but possible.

Cyrix Reaches 0.44 Microns

To achieve 150 MHz operation, Cyrix, along with fab partner IBM, developed a 0.44-micron version of the 6x86 built in a variant of IBM's CMOS-5S process called CMOS-5S2. This device is a 10% optical shrink of the 0.5-micron version

currently shipping at 133 MHz (see MPR 2/12/96, p. 11). The new die measures 169 mm^2, 18% smaller than the previous version. The MDR Cost Model estimates the new manufacturing cost at $75, 12% less than before.

Cyrix plans to move most of its production to the shrunk part, which also improves yield at the lower frequencies while reducing cost. The 6x86 remains far more expensive to produce than Pentium, which we estimate costs just $40 to manufacture. By focusing its efforts on products that sell for $300 and up, however, Cyrix makes this cost difference acceptable.

Cyrix has priced its 6x86-P200+ at $499 in quantities of 1,000. IBM is also selling the P200+ under its own label, at a 1,000-piece list price of $479. These prices are 20% or more below Intel's Pentium-200 price, but this gap is not really meaningful. Intel is scheduled to reduce its prices on July 29, about the time the P200+ reaches volume production; we expect the Pentium-200 will be much closer to Cyrix's $499 price by the time most vendors can buy the 6x86.

Cyrix is also working with its second foundry partner, SGS-Thomson, which has not yet been able to ship any 6x86 parts in volume. SGS-Thomson's Phoenix (Ariz.) fab is now producing samples of the 6x86, and the vendor expects to put these parts into production in 2H96.

As part of its system effort (see MPR 4/15/96, p. 4), Cyrix is selling 6x86-P200+ PCs, promising shipments by the end of this month. The base price for these systems is $2,699 in a configuration that includes a 256K pipeline-burst cache, 16M of EDO memory, a Matrox Millennium graphics card with 2M of WRAM, 2.5G hard drive, 8× CD-ROM, 15-inch monitor, speakers, and Windows 95.

Cyrix measured a high-end configuration, which included a 4G SCSI-2 disk with 64M of cache, at 100.5 on the Winstone 96 benchmark. This score is the highest ever published on that metric, including ratings for Pentium and Pentium Pro systems, although Pentium Pro might do better if tested with such a disk controller. Cyrix's record-breaking configuration is on the price list at $4,999.

Cyrix M2 to Duel Klamath

In early 1997, Cyrix plans to debut its next design, code-named M2. This device will retain the proven 6x86 processor core but quadruple the size of that chip's unified L1 cache to 64K, twice as much on-chip cache as the P55C. The greatly expanded cache will help overcome the bandwidth limitations of the Pentium bus.

Combined with the greater efficiency of the 6x86 CPU core, the new cache should help the M2 achieve better performance than the P55C. Sticking with the current pinout provides PC makers the option of extending the lifetime of their Pentium-based motherboards by moving to the M2.

The M2 will debut in IBM's 0.35-micron CMOS-5X process, which should allow clock frequencies of 180 and 200 MHz. We expect a subsequent shrink to the 0.27-micron CMOS-6S process in 2H97, boosting M2 speeds to 225 and 250 MHz; these parts would use a 75- and 83-MHz bus, respectively, for best performance. If Cyrix can deliver parts on this timetable, the M2 should be comparable in 16- and 32-bit integer performance to Intel's Klamath, a P6-family part expected to roll out early next year.

We believe the performance of the 6x86 core will begin to suffer at speeds above 200 MHz, even with the larger cache, due to the limited bus bandwidth. Cyrix, within the Pentium pinout, will find it difficult to match the performance of Intel's 300-MHz P6 (code-named Deschutes), expected to ship by the end of 1997. The 6x86 core might deliver better performance by moving to a new pinout, perhaps retaining the Pentium bus interface but adding a new L2 cache bus. Cyrix, however, does not expect to adopt a new pinout until its M3 processor, due in 1998.

Price & Availability

Intel's 200-MHz Pentium is available now at a 1,000-piece list price of $599. For more information, contact your local Intel sales office or check the World Wide Web at *www.intel.com*. For specific information on the plastic PGA package, request document 243103-001 from the Intel Literature Center at 800.548.4725.

The 6x86-P200+ is available in limited quantities now, with volume production slated for early August from both Cyrix and IBM. Cyrix's list price is $499 in quantities of 1,000. IBM's price is $479 in the same quantities.

Contact Cyrix (Richardson, Texas) at 214.968.8388; fax 214.699.9857 or check the Web at *www.cyrix.com*. Contact IBM Microelectronics through its fax-back service at 415.855.4121 or via the Web at *www.chips.ibm.com*.

Cyrix Adopts MMX

A key enhancement of Klamath over Pentium Pro is the addition of MMX support. To match Klamath, Cyrix has added MMX to the M2 as well. The company had initially developed its own set of multimedia instructions for M2, but when both Intel and AMD adopted MMX, Cyrix realized it had no choice but to offer compatible instructions. The company says converting to MMX added only 30–60 days to the M2 schedule, a small price to pay for compatibility.

Unlike AMD, Cyrix has not licensed MMX from Intel. From a legal standpoint, Cyrix's ability to implement these instructions should be no different from its current implementation of other x86 instructions. Presumably, its use of Intel-licensed foundries—IBM and SGS-Thomson—should protect its MMX designs.

Cyrix based its MMX implementation on public information about the new instructions. It remains to be seen whether this implementation will be fully compatible with Intel's. When Cyrix delivered its first Intel-compatible processor, the x86 instruction set had been relatively well

	Intel Pentium		P200 vs. P166	6x86 150 MHz	6x86 vs. P200
	166 MHz	200 MHz			
Winstone 96	**81.5**	**89.0**	**9.2%**	**91.6**	**2.9%**
Graphics	8.0	8.6	7.5%	8.7	1.2%
Database	9.3	10.2	9.7%	10.5	3.6%
Spreadsheet	7.5	8.2	9.3%	8.5	3.7%
Word Proc.	8.2	9.0	9.8%	9.3	3.0%
Winstone 32	**107.7**	**114.8**	**6.6%**	**120.6**	**5.1%**
Graphics	9.3	9.7	4.3%	9.9	1.7%
Database	13.5	14.7	8.9%	15.4	4.3%
WP/SS	10.6	11.4	7.5%	12.2	6.4%

Table 1. Cyrix's 6x86-P200+, which runs at 150 MHz, slightly outperforms Intel's Pentium-200 on PC application benchmarks. See article text for configuration details. (Source: MDR Labs)

documented for years. The startup discovered several "holes" in this documentation only through extensive testing of Intel's own processors, and since then the Cyrix designs have had no significant compatibility issues.

Bringing out its MMX processors just a few months after Intel's raises the level of risk. Cyrix will have little, if any, opportunity to test Intel's MMX processors before finalizing the M2. Without this testing, the possibility of a compatibility problem is greater. MMX is much simpler than the rest of the x86 architecture, however, minimizing this risk.

Another issue for Cyrix is that it will have no MMX-enabled part that matches well against the P55C. The M2 should exceed the performance of the P55C, positioning it against Klamath. That would leave the current 6x86 to take on the P55C. If the market demands MMX at the P55C price points, Cyrix may choose to offer low-speed versions of the M2 instead. By 2H97, however, P55C prices will fall below $300, removing this problem from Cyrix's radar screen.

Cyrix Gains on 16-Bit and 32-Bit Applications

MDR Labs measured the performance of both the 200-MHz Pentium and 150-MHz 6x86 on two PC application suites: Ziff-Davis's Winstone 96 and new Winstone 32. Winstone 96 is a popular metric that consists of a variety of 16-bit PC applications that we ran under Windows 95. Winstone 32, which we also ran under Windows 95, contains only 32-bit (Win32) PC applications.

Because the two chips use different system bus speeds, it was impossible to run them in the same motherboard for the best comparison. We tested the 6x86 in a DFI board using the Lynx chip set, which is the only available chip set that supports a 75-MHz bus. Although this board can be configured at 66 MHz for the Pentium-200, we measured the Intel chip in a Tyan motherboard using Intel's 430HX (Triton II) chip set, which delivers better performance than Lynx for the Pentium processor. For comparison, we also tested a Pentium-166 in the same Tyan motherboard.

Other than these differences, the two test systems were as identical as possible. They both included 256K of pipeline-burst cache, 32M of EDO DRAM, a Seagate Barracuda 2G disk connected through an Adaptec SCSI adapter, and a Matrox Millennium graphics card with 2M of WRAM. Measurements were taken with the graphics card set for 1024 × 768 × 8-bit resolution.

The data in Table 1 shows the 150-MHz 6x86 outperforms the 200-MHz Pentium by 2.9% on Winstone 96 and 5.1% on Winstone 32. The Cyrix chip consistently outscores the Pentium, coming out ahead on every component of each metric. Except for the business-graphics component in both suites, the Cyrix chip wins by 3.0–6.4%. (A complete report is on the Web at *www.chipanalyst.com.*) None of these tests contains significant amounts of floating-point code, on which the 6x86 is slower than Pentium.

End users are unlikely to perceive such small differences in performance. But given the relatively small gap between the performance of the Pentium-200 and the Pentium-166, the 6x86's edge appears more significant, particularly on 32-bit code.

Cyrix Strategy Raises Socket Issues

Over the past few months, Cyrix has demonstrated that its 6x86 can match Intel's fastest Pentium on mainstream PC applications, and the company has responded well to Intel's first attempt to restore a performance gap. We expect Cyrix to continue to stay close to the PC application performance (except for 3D graphics) of Intel's top parts for at least the next year, moving to the M2 as Intel moves to Klamath.

A key difference between these two P6-class parts will be the pinout. Both Cyrix and AMD will try to extend the performance range, and thus the life, of the P55C socket with the M2 and K6, respectively. Staying with the P55C socket will help PC makers in the short term, but moving to the Klamath pinout will provide much more performance headroom in the long term. Intel's competitors were successful with the 486 pinout in 1995 but not 1996; we expect the P55C pinout to be successful in 1997 but less so in 1998.

Although matching Intel's fastest Pentium is a big PR boost for Cyrix, the most important effect of the new version of the 6x86 is increasing yield and reducing the cost of the P133+, P150+, and P166+ versions, which sell into segments of the market with higher volumes than the P200+. Even as the P200+ declines in price, we do not foresee significant sales, even by Cyrix standards. Although the P200+ is nominally pin-compatible with Pentium, its 75-MHz bus makes it incompatible with all current Pentium motherboards. We expect few vendors to redesign boards for the 6x86-P200+, limiting its adoption.

In contrast, the Pentium-200 offers an easy upgrade to existing motherboards. For the next several months, the new clock speed will be the high end for consumers and others who don't want Pentium Pro. In fact, Intel doesn't expect P55C systems to be in stores in time for Christmas, leaving the Pentium-200 as the premium model through the holiday buying season. Once P55C ships in volume, however, the Pentium-200 will be a quickly fading memory. M

401GF Is Coolest, Cheapest PowerPC

IBM's Low-Power Processor Delivers 650 MIPS/Watt with a $13 Price Tag

by Jim Turley

For the first time, PowerPC chips can mount a credible assault on the market for low-cost battery-operated devices. Fulfilling a year-old promise, IBM Microelectronics rolled out its PowerPC 401 core, providing a new low end to the PowerPC family. The small new design maintains software compatibility with the range of PowerPC processors from IBM and Motorola but drops prices below $15.

At 25 MHz, the part merely sips power, consuming just 40 mW (typical) from a 2.5-V supply—one-fifth the power of previous embedded PowerPC chips and well into the target range for portable devices.

The 401 core is available both as a macrocell for ASIC development and as a packaged part, the 401GF. At $13 in quantity, the 401GF is the least expensive PowerPC chip made, yet it delivers 52.5 Dhrystone MIPS at 50 MHz. The 25-MHz and 50-MHz versions of the 401GF will begin sampling in a few weeks; 75- and 100-MHz versions will follow before the end of 1996, according to IBM.

Stripped to the Core

The 401GF achieves its remarkably low power consumption through a combination of design tradeoffs, circuit-design techniques, and fabrication process. As IBM's entry-level PowerPC, the 401 core includes only the features absolutely necessary for PowerPC compatibility. For example, the 401GF does not include the serial ports, MMU, DRAM controller, or DMA logic of the earlier 403-series parts (see MPR 5/9/94, p. 1). As Table 1 shows, the 401GF includes little more than a 401 core, dual caches, and a multiplexed bus interface.

By its nature as a PowerPC implementation, the 401GF has a somewhat richer feature set than most minimal embedded CPUs. For example, the chip supports simple static branch prediction, handles unaligned loads and stores, offers selectable byte ordering, includes a hardware multiply and divide unit, and has separate instruction and data caches. The 401's register file is triple ported, reducing pipeline stalls and contention for the internal buses.

The caches are more deluxe than usual for a low-cost chip. The data cache has a two-line write buffer, both caches can be locked on a line-by-line basis, and both forward the critical word first. In all, these features help the 401GF attain its 1.05 MIPS/MHz ratio. They also contribute to its relatively bulky die size.

Processor	401GF	403GA	403GB	403GC
Max freq	50 MHz	33 MHz	28 MHz	33 MHz
I/D cache	2K/1K	2K/1K	2K/1K	2K/1K
Dhry MIPS	52 MIPS	41 MIPS	35 MIPS	41 MIPS
Voltage	3.3 V	3.3 V	3.3 V	3.3 V
Power (typ)	140 mW	265 mW	200 mW	200 mW
Package	TQFP-80	PQFP-160	TQFP-128	PQFP-160
MMU?	No	No	No	Yes
DRAM ctrl?	No	Yes	Yes	Yes
DMA chan	None	4	2	4
Serial chan	None	1	1	1
Availability	2Q96	Now	Now	Now
Price (10K)	$13	$28	$25	$30

Table 1. The 401GF is similar to IBM's three 403-series parts in many respects, including the caches, but without the peripherals.

Optimized for ASICs

The first two versions of the 401GF, at 25 and 50 MHz, are fabricated in IBM's 0.5-micron three-layer-metal CMOS-5S process. At 4.5 mm^2, the 401 core is hardly oversize, but the inherent complexity of the PowerPC architecture does tip the scales a bit. The notoriously small ARM7 core, for instance, measures just 3.8 mm^2 in a less aggressive 0.7-micron process. LSI Logic's CW4001 covers 3.5 mm^2 in a comparable 0.5-micron process, less one metal layer. In IBM's favor, though, neither of these cores offers any of the performance features mentioned above.

IBM's design method is tailored for ASICs, even on its standard parts. Although not immediately clear from the die photo in Figure 1, the 401GF has two internal buses—one for low-latency units close to the CPU core and another for relatively long latency peripherals—with a bus bridge between them. Since the 401GF has no on-chip peripherals, the secondary bus sits unused; on its 403-series brethren, it hosts the serial channels. IBM is studiously building its library of peripheral functions, hoping to attract PowerPC-based ASIC customers that Motorola cannot service.

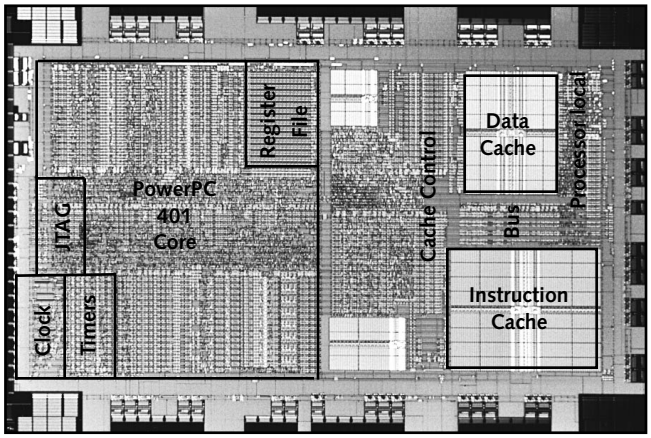


Figure 1. The 401GF is laid out for convenient ASIC development, so less than 25% (4.5 mm^2) of the chip's 22 mm^2 is dedicated to the PowerPC core in IBM's 0.5-micron three-layer-metal process.

Price & Availability

IBM's 401GF is sampling now in an 80-lead TQFP package; 75- and 100-MHz samples will be available near the end of 1996. In 10,000-piece quantities, the 401GF is priced at $13. For more information, contact IBM Microelectronics (Research Triangle Park, NC) via fax at 415.855.4121, or visit IBM's embedded PowerPC page at *www.chips.ibm.com/products/embedded/index.html*.

Conditional Clocking Quiets 401's Logic

The 401's three-stage pipeline is the minimum necessary for a contemporary RISC design, yet it allows the chip to reach competitive performance levels: IBM expects to sample the 75-MHz version before the end of the year and, with a possible process shrink to 0.35 micron, a 100-MHz chip. The ARM7 core, in contrast, is currently limited to 40 MHz without expanding its three-stage pipeline into five stages.

The 401GF relies heavily on conditional clocking and clock-distribution tricks. Individual sections of the 401 core are clocked only as necessary, with registers, execute stages, and buffers idled when not in use. The 401GF also has four user-selectable power-down states, from wait mode, which stops fetching and cuts power in half, to deep sleep, which halts all circuits while power consumption plummets to just 0.015 mW. Resuscitating the 401GF from deep sleep requires a hardware interrupt and a good 1.5 milliseconds, or 37,500 cycles at 25 MHz.

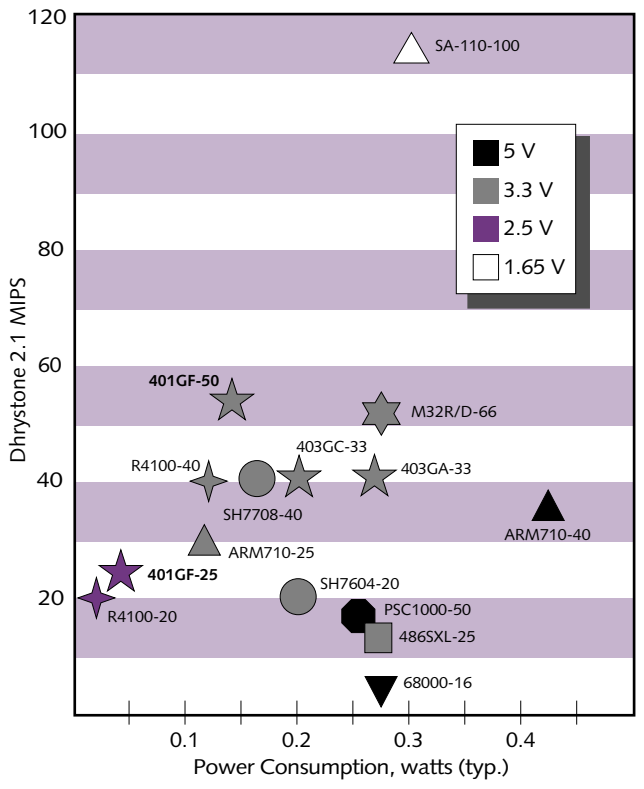


Figure 2. The 401GF's low power consumption compares favorably with that of a number of other recently announced embedded microprocessors. (Source: vendors)

Good for Low Power

The chip's estimated power consumption is impressively low. At 25 MHz, the 401GF draws about 16 mA from its 2.5-V supply, for 40 mW of typical power consumption. At 656 MIPS/watt, the 401GF unseats even the impressive StrongArm-110 (see MPR 2/12/96, p. 1) in power/performance efficiency, though it comes nowhere near the Digital chip's high-end performance. As Figure 2 shows, the 401GF comes in a close second behind NEC's 20-MHz R4100 (see MPR 3/27/95, p. 12), which, at just 27 mW and 20 MIPS, stands out with an amazing 815 MIPS/watt.

The 401GF can operate up to 25 MHz at 2.5 V; after that, a 3.3-V supply is required. The higher supply voltage has the side effect of giving the chip compatibility with conventional 5-V I/O levels.

Turning up the clock frequency on the puny PowerPC increases performance linearly, but its power consumption climbs even faster because of the jump to 3.3 V. At 50 MHz, the 401GF needs closer to 140 mW, dropping its MIPS/watt ratio to about 375—still an efficient part. At 100 MHz, the 401GF will give the 100-MHz SA-110 a run for its money, coming within a few percent of Digital's estimated integer performance and power consumption—and all from a 3.3-V supply, twice the voltage of the SA-110 core.

The economic ratios are just as good. IBM is pricing both the 25-MHz and the 50-MHz versions of its new chip at $13 in 10,000-unit quantities. These prices are less than half that of the cheapest SA-110 and cheaper than the R4100's. The 401 challenges low-cost products like Hitachi's SH-3 family and NEC's V800 line. Unlike those architectures, PowerPC has a broad, clear upgrade path to higher performance and (at least in the midrange) an alternate vendor.

IBM Picking Up Speed in Embedded Market

IBM has come a long way since the company began its embedded PowerPC line two years ago. Although the chips in IBM's embedded line were sometimes hard to tell apart, the company is now beginning to grow into a full-line microprocessor supplier. For the next few years, IBM will continue to emphasize its core-based ASIC capabilities rather than its thin catalog of standard designs. The ASIC designs will fill the fabs and cover the time the company needs to assemble a credible array of standard peripherals.

For consumer-electronics and portable-communications-gear makers with the wherewithal for ASIC development and a taste for PowerPC, IBM is the obvious choice. But even without the "brand name" recognition of the world's best-selling desktop RISC processor, IBM has created a very competitive 32-bit embedded CPU that stacks up well against the best. M

AGP Speeds 3D Graphics

Accelerated Graphics Port Enables New Generation of 3D Accelerators

by Yong Yao

Continuing to set new standards in PC system design, Intel unveiled the details of its proposed accelerated graphics port (AGP) architecture at the recent AGP conference. The new interconnect addresses latency and bandwidth limitations that arise when PCI is used for 3D graphics. AGP is an extension of the basic PCI architecture, but it adds a demultiplexed address bus, pipelined transfers, and a 133-MHz effective transfer rate to improve performance.

This increased performance enables 3D texture data, traditionally kept in the frame buffer, to move to main memory. This change makes memory usage more efficient and frees frame-buffer bandwidth for tasks such as screen refreshing and Z-buffering. Besides helping 3D performance, AGP will also boost 2D performance due to the lower arbitration overhead and the higher data rate among the graphics controller, CPU, and main memory.

To achieve the high transfer rate, AGP is defined as a point-to-point connection, not a bus. While this design simplifies the electrical environment, it implies that the graphics subsystem be connected directly to the system-logic chip set; no other devices in the system can use AGP. A system can include an AGP-based graphics controller on the motherboard, or it can include a single AGP slot for an add-in graphics-accelerator card.

As it did with PCI and USB, Intel is aggressively pushing AGP into the PC market. The company has already signed Microsoft as well as a slew of graphics vendors to back the new standard, which Intel is openly licensing. The first AGP chip sets and graphics cards are due to appear in 1H97; by the end of next year, AGP should be in many high-end systems, becoming widely used within two to three years.

High-performance 3D graphics will be one of the key areas driving PC performance over the next several years. Intel realized that the basic PC architecture of today must be modified to deliver optimal 3D performance and thus has offered AGP as a solution. The company is also leaping into the 3D chip market; its first such product, due next year, will be an AGP-based 3D accelerator.

Resolution	Screen refresh 75 MHz	Color plane (R/W)	Z-buffer	Texture	Other	Total bandwidth required
640 × 480	50	100	100	100	20	370
800 × 600	100	150	150	150	30	580
1024 × 768	150	200	200	250	40	840

Table 1. 3D rendering bandwidth requirements in Mbytes/s. The numbers are based on 16-bit color, 30 frames per second, and average scene complexity (average amount of polygon overlap) equal to three.

Texture Maps Overwhelm PCI

Not long ago, PCI was created to resolve the data-bandwidth problem among peripherals, memory, and the host CPU. Ironically, the bandwidth of the PCI bus has now become the bottleneck in some advanced PC designs for 3D graphics. Rendering in 3D requires a large amount of bandwidth between the graphics accelerator and the frame buffer, as Table 1 shows. To meet these bandwidth requirements, many graphics subsystems use expensive high-performance memory chips, increasing the cost of the system.

One way to ease this problem is to move texture data from the frame buffer to main memory, as Figure 1 shows. Texture data is a good candidate to make this move for several reasons. First, it is generally read only; moving it to main memory does not cause data-consistency problems. Second, texture data must pass through main memory when it is loaded from mass storage; leaving it in main memory actually reduces overhead. Finally, texture size will grow as 3D applications become more complex and deliver better image quality, so leaving textures in the frame buffer will continue to increase the graphics subsystem cost over time.

Moving texture data to main memory reduces the size, and thus the cost, of the frame buffer, but it requires a corresponding amount of storage in main memory. From a system perspective, however, it is better to increase the size of main memory than of the frame buffer, because main memory uses less expensive DRAMs. In addition, storing texture data in main memory improves memory utilization, because application-dependent textures can be returned to the free memory heap when the application completes.

Unfortunately, this move shifts the bandwidth pressure from the frame buffer to the PCI bus. As Table 1 shows, texture data alone will exceed today's PCI bandwidth limit of

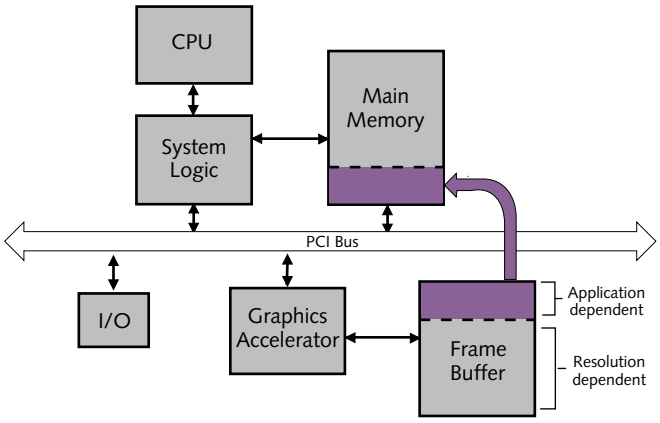


Figure 1. Moving texture data from the frame buffer to main memory can reduce the cost of the graphics subsystem, but the texture data requires more bandwidth than PCI can deliver.

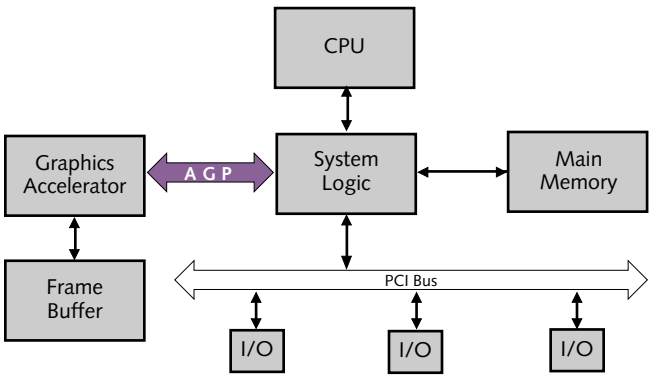


Figure 2. The proposed AGP system architecture adds a high-bandwidth path between the graphics subsystem and the system-logic chip set but has no impact on any other I/O subsystem.

100 Mbytes/s. Thus, a new method of connecting graphics to main memory is required.

AGP Extends PCI Standard

The primary goal of the AGP initiative is to contain the cost of implementing 3D in PCs while enabling performance improvements. Intel has made three major extensions to PCI for the AGP interface:

- Deeply pipelined memory read and write operations
- 133-MHz data-transfer rates
- Demultiplexing of address and data

These changes provide bandwidth and latency improvements well beyond that of the current 32-bit 33-MHz PCI bus and beyond even what the 66-MHz 64-bit PCI specification provides.

Signal name	Function description
IRDY#	Indicates the master is ready to provide all write data for the current transaction.
TRDY#	Indicates the target is ready to provide read data for a whole 32-byte block.
GNT#	Same meaning in AGP as in PCI, but additional information is associated with it.
C/BE[3:0]	Provides command information (different than PCI) when requests are being queued.
PIPE#	Used to queue pipelined request using the AD bus.
SBA[7:0]	Additional bus to queue pipelined requests.
SBE	Enables the SBA bus to be used.
ST[2:0]	Indicates how the AD bus will be used next.
AD_STB	Indicates the AD bus has valid data (2× mode).
SB_STB	Indicates the SBA bus has a valid request (2× mode).
DBF#	Indicates if the master can accept normal-priority read data.

Table 2. The first set of signals have a different meaning in AGP than in PCI; the second set are the 16 new AGP signals that are not part of the PCI specification. In the table, the master refers to an AGP-compliant graphics controller and the target refers to an AGP-compliant system-logic chip set.

Given these differences, Intel attempted to leverage as much of the PCI specification as possible. The three AGP performance enhancements are realized though the use of "sideband" signals, which are separate from the standard PCI signal set. AGP specifically avoids the use of any of the reserved fields, encodings, and pins in the PCI specification. AGP-defined protocols like pipelining are overlaid on PCI in such a manner that a standard PCI-compliant agent would view the bus as idle.

Despite these similarities, AGP and PCI devices cannot coexist. The key reason is that AGP is not a bus; it supports only a single device. Intel could have attempted to build AGP as a precise superset of PCI, putting AGP devices on that bus, but this decision would have either restricted AGP to 33 MHz or forced all PCI devices to support a 66-MHz clock, a needless cost burden for most PCI peripherals. In addition, AGP defines a different connector than PCI; the demultiplexed address signals would not fit in the current PCI connector. Thus, AGP devices need to be off of the PCI bus.

Leveraging the PCI definition allowed Intel to develop the AGP specification more quickly; the very concept of AGP did not exist until six months ago. The similarities to PCI will also ease the task of hardware designers. For the next few years, many graphics chips are likely to sport a dual AGP/PCI interface, allowing the system designer more flexibility. In fact, some the first "AGP" graphics chips may simply be slightly modified PCI chips that do not support many of the optional features of AGP.

AGP Boosts Memory Bandwidth

AGP is defined as a point-to-point connection based on a 3.3-V 66-MHz PCI bus. As Figure 2 shows, at one end of the connection is a device called the AGP-compliant target, which must always be the main-memory controller. The memory controller is part of the system logic in today's PCs.

Cycle name	CBE# status	Cycle description
Read	0000	Read n sequential Q-words, where n=length_field+1*.
Priority read	0001	Same as Read, but the request is queued in the high priority queue.
Write	0010	Write n sequential Q-words, where n=length_field+1*.
Priority write	0011	Same as Write, but indicates that the write data must be transferred from the master within the maximum latency window established for high-priority accesses.
Long read	1000	Same as Read except for access size, in this case n=4* (length_field+1), allowing up to 256-byte transfers.
Priority long read	1001	Same as Priority read except for access size, in this case n=4* (length_field+1), allowing up to 256-byte transfers.
Flush	1010	Similar to read. This command drives all accesses ahead of it to the point that all the results are fully visible to all other system agents, and then returns a single Qwork of random data as an indication of its completion.
Fence	1100	Creates a boundary in a single master's access stream, around which writes may not pass reads. This command does not occupy a slot in the AGP pipeline.

Table 3 The CBE lines provide bus commands for AGP pipeline operations. *The length_field is specified by the SBA bus.

At the other end is the AGP-compliant master, which is a graphics accelerator. The point-to-point connection not only makes the double-edged clocking possible, it also improves data integrity, simplifies the AGP protocols, and eliminates PCI bus arbitration overhead.

The AGP interface closely resembles that of the PCI bus. Most PCI signals are reused in AGP transactions, while others have slightly different semantics, as Table 2 shows. There are 16 new signals, also listed in Table 2, defined by the AGP specification. The PCI FRAME#, DEVSEL#, STOP#, and IDSEL signals are not used during AGP transactions. All AGP devices, however, are also required to respond to PCI transactions, so they must handle these signals as defined by the PCI specification.

Pipelining Improves Read Operations

Pipelining is the major protocol enhancement provided by AGP. Only memory read and write operations targeted to main memory are affected by pipelining. All other bus operations, including reads and writes to the graphics controller, are executed as standard PCI transactions. The request portion of an AGP transaction is signaled differently than a PCI address phase. The information is still transferred on the AD and C/BE# signals of the bus, as is the case with PCI, but is identified with the new signal PIPE# instead of FRAME#.

The system logic can access the graphics chip only with PCI transactions. Only the graphics chip can use pipelined transactions while accessing main memory. Table 3 lists the AGP pipeline operations. Note that, unlike PCI transactions, AGP pipeline transactions are not cache coherent and cannot be retried or terminated after they start.

The pipelined transactions defined by AGP run in a split-transaction fashion. The graphics chip initiates a pipelined transaction with an access request. The system logic responds to the request by initiating the corresponding data transfer at a later time. The graphics chip can then issue its next pipelined transaction while waiting for the previous data to return. This overlap results in several requests (reads or writes) active in the target's request queue at any point in time. The AGP specification does not impose a limit on how many outstanding transactions are allowed; this limit is determined by individual implementations.

As Figure 3 shows, the request queue is divided into high-priority and normal-priority subqueues, each of which deals with respective accesses according to its own rules. Data within a given queue is always returned in order, but data from different queues may be returned out of order. Figure 4 shows a transaction example.

Double Clocking Allows 133-MHz Transfer Rate

Another significant change between AGP and PCI is the double-clocking technique used to achieve a 133-MHz data transfer rate. The AGP interface operates with a 66-MHz clock, but data can be transferred on both clock edges. Most of the AGP electrical interface specifications are based on 66-

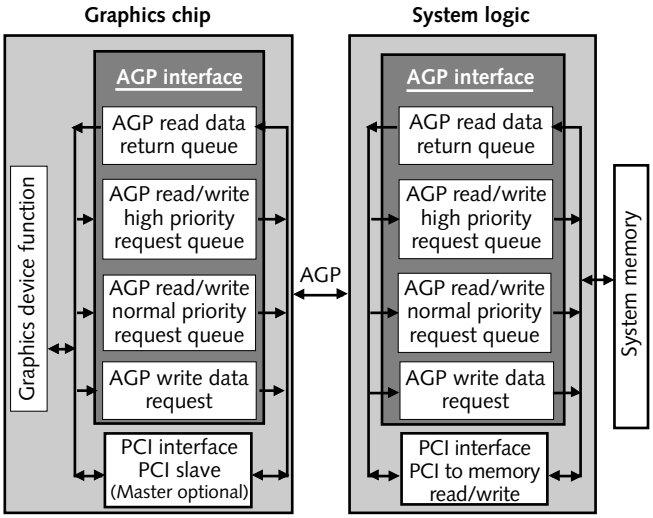


Figure 3. To improve response time, AGP's access queuing model divides transactions into high and normal priorities.

MHz PCI, but AGP has two transfer modes: 1× and 2×. Because it is a point-to-point connection using 3.3-V signaling, the AGP specification for the 1× transfer mode actually relaxes some of the design specifications relative to 66-MHz PCI. The 2× transfer mode, referred to as AGP-133, requires additional interface timing strobes and different signal timings from the 1× mode.

With a 133-MHz effective transfer rate, AGP reaches 533 Mbytes/s of peak bandwidth. In addition, its sustained bandwidth is significantly improved over PCI's by pipelining and demultiplexing.

Sideband Port Demultiplexes Address

To further increase the efficiency of the AGP interface, especially for random memory accesses, Intel added a sideband address (SBA) bus. This bus demultiplexes the address of an AGP transaction from the data. It is used exclusively to transmit AGP access requests. Therefore, it is always driven from

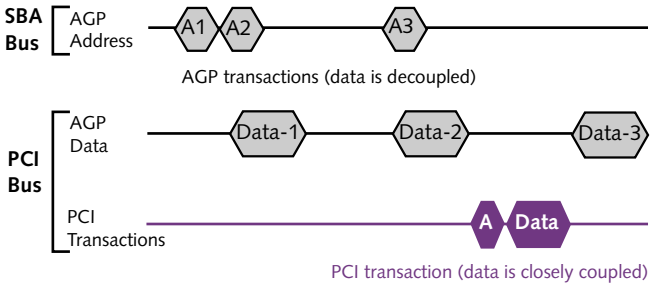


Figure 4. Sample AGP transactions show the PCI address phase and its corresponding data are always together. For a pipelined AGP transaction, the address phase and data phase are decoupled. In the figure, the PCI transaction is running out-of-order with the third AGP transaction. Note that pipelined transactions can also be performed without the optional SBA bus.

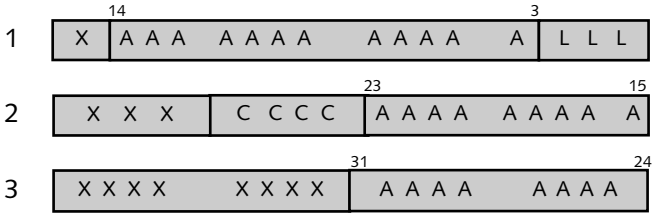


Figure 5. Address (A), command (C), and length (L) bits are transferred across the sideband address bus in three groups, as shown. Each group requires two 8-bit transfers.

the master to the target. Since use of the SBA bus indicates a pipelined transaction, there is no need for the PIPE# signal. Supporting SBA is optional for the master, but an AGP-compliant chip set is required to support this bus. If an AGP master uses the SBA bus, it will always issue demultiplexed transactions.

The sideband address bus (SBA[7:0]) is only 8 bits wide, reducing pin count. To use this bus, a complete AGP request is broken into three parts: low- order address bits and length, middle address bits and command, and high-order address bits, as Figure 5 shows. Each of these three parts takes two 8-bit transfers, or one cycle when double clocking. The latter two parts of the request need be transmitted only if they have changed since the previous request, which exploits potential locality among requests to minimize traffic over the SBA bus.

AGP Requires Address Remapping Table

Texture maps that are stored in main memory must be contiguous from the point of view of the application and the 3D controller. A typical 256 × 256 pixel 16-bit texture map is 128K in size, but Windows cannot allocate that much contiguous physical memory. Intel's solution is to have Windows allocate space for texture maps in the application's virtual address space, then lock the pages into physical memory. This method results in each texture map occupying many 4K pages distributed throughout physical memory.

Intel's AGP chip set contains a graphics address remapping table (GART) that mimics this virtual-to-physical address translation. Accesses from the graphics controller to a special address range are translated by the GART into physical addresses, making the textures appear to be contiguous. The GART is potentially quite large. A 4M window requires a 1024-entry GART, with each entry occupying 4 bytes.

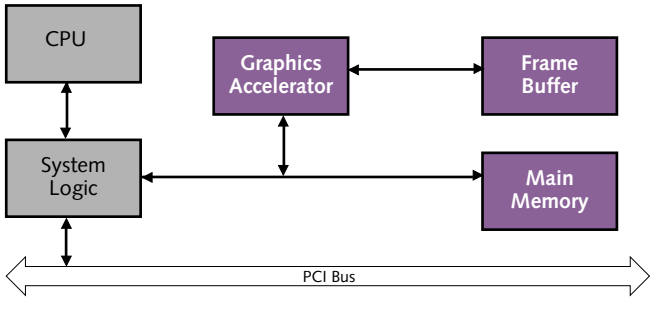


Figure 6. VESA has defined a version of its UMA design that places the graphics accelerator and its frame buffer on the main-memory bus.

The AGP specification does not describe how the GART is to be implemented by a chip set vendor. Instead, the vendor must provide a chip set driver that manages the GART according to a GART Services API that will be defined in the AGP specification. This definition should allow vendors other than Intel to design AGP chip sets that are compatible with Intel's at the operating-system level. The detailed definition of the GART and the API is not yet available, and this may delay third-party chip-set designs slightly.

Intel will be the first to market with an AGP chip set. This chip set, known as the 440LX, is designed for P6 (primarily Klamath) systems. Intel says it will not develop AGP chip sets for Pentium (including P55C) systems, although the P55C will still be the major volume player when AGP debuts; this decision is apparently a ploy to motivate home users to move to Klamath. We expect other vendors to add AGP to their Pentium and P6 chip sets, although they may lag Intel to market by three to six months.

A well-designed system-logic chip set is critical to bring the AGP architecture into full play. The chip set must bring the graphics accelerator logically closer to the host CPU and handles concurrent operations among the CPU, the graphics accelerator, main memory, and PCI masters. Even when multiple AGP chip sets are available, they may be significant performance differences among them.

UMA Offers Product Differentiation

The Video Electronics Standards Association (VESA) had also foreseen the increase in bandwidth needed for efficient 3D performance. As part of its UMA standard, VESA defined an optional method of connecting the graphics controller, frame buffer, main-memory controller, and main memory all across a high-bandwidth memory bus, as Figure 6 shows. This design allows the graphics controller to freely access either the frame buffer or main memory without requiring any intervention from the system logic; a simple handshaking protocol controls access to the memory bus.

The VESA proposal has some technical advantages:

- It adds only a couple of control lines to the chip set and the graphics accelerator, reducing the cost of manufacturing the chip set.
- It provides a 64-bit connection to memory, twice the width of AGP's. The interface speed will grow with memory technologies. For instance, today's fast SDRAM can operate at 100 MHz or higher.
- The graphics accelerator can directly access main memory without a chip set in between.

AGP, however, has its own technical advantages:

- The AGP interface is independent of the memory technology used for main memory.
- The chip set sees every access to main memory and can

For More Information

For more information on AGP, contact the AGP Implementors Forum at 503.264.9222; fax 503.264.5959 or access the Web at *www.teleport.com/~agfxport*.

allocate valuable memory bandwidth most efficiently.

• AGP does not impart an additional load on the system-memory interface.

• Unlike the VESA proposal, AGP can support both add-in graphics cards and motherboard implementations.

The VESA proposal illustrates a different technical approach to the bandwidth problem, but ultimately the important differences between the two proposals are the industry backers. The backing of Intel and Microsoft, along with a large number of graphics vendors, ensures AGP's success. Just as PCI outmuscled VESA's VL-bus, AGP will even more easily brush aside this alternative proposal.

AGP Headed for Rapid Acceptance

AGP is an open specification, in that it will be licensed to all interested parties under royalty-free reciprocal terms, similar to USB. Unlike USB, the definition of AGP is controlled by Intel alone. Because of this, the definition of AGP has been completed much more quickly than with USB or PCI. All major 3D graphics companies, such as 3Dfx, 3Dlabs, ATI, Cirrus Logic, Rendition, S3, and Trident, plan to support AGP. Intel expects to ship its first AGP system-logic chip set in 1H97. In the same time frame, some of the early adopters will launch their AGP-compliant graphics accelerators.

AGP is not an all-purpose solution. It does not, for example, solve the problem of making PCI faster; for most nongraphics devices, however, the current PCI definition is quite adequate. In fact, graphics was the key driver behind the 66-MHz 64-bit PCI standard; with AGP, it is now unlikely that this PCI extension will be implemented. Another issue is cost. The double-edge transfers require a more precise clock signal. Because of this, both the graphics chip and the system logic may need built-in PLL circuitry, which increases the manufacturing cost of the two devices.

Another issue is software support. To take advantage of an AGP (or UMA) design, either the device drivers or the operating system must support dynamic memory allocation. Windows 95 does not have this capability today, but Microsoft plans to fix this problem by the end of this year.

With its broad industry support, there is no doubt AGP will do well. Intel projects AGP penetration will reach about 90% by the year 2000, a ramp rate similar to that of PCI. With both Intel and Microsoft backing the idea, and a slew of graphics makers on board, AGP has enough momentum to be a sure winner. Graphics and system-logic vendors should plan accordingly. M

Intel to Enter 3D Chip Market

Intel has teamed with Lockheed-Martin to develop a 3D graphics accelerator based on AGP. Intel is not currently in the graphics chip market. The new device is based on Lockheed's 3D aviation simulations; both Intel and Lockheed will sell the new device.

Slated for introduction in the second half of 1997, the Intel 3D graphics accelerator will be an AGP-compliant master for Klamath systems. Theoretically, any AGP graphics accelerator is CPU independent, because it is decoupled by the AGP port, but of course it requires AGP-compatible system logic. Its performance is very chip-set dependent, while the chip set is CPU specific. The jointly developed accelerator will probably integrate 2D graphics, a RAMDAC, and video acceleration along with 3D functions.

We expect the device will rely on the host processor to do geometry calculations such as rotating, scaling, translation, lighting, clipping, and culling. The accelerator will handle setup and rendering. Additional features expected in the Intel graphics accelerator include:

- A single-chip solution based on the unified buffer architecture, with texture maps in main memory
- Support for Z-buffer, texture MIP mapping, perspective correction, Gouraud and Phong shading, anti-aliasing, alpha blending, stencil and scissor testing, and stipple masking
- Optimizations for the Klamath processor, Intel's Klamath (440LX) chip set, and Microsoft's Direct3D API
- A performance target of 30–50 million pixels per second and 500,000–1,000,000 50-pixel triangles per second, where pixels are textured and bilinear filtered

The graphics market is a natural extension of Intel's business. Intel is a giant semiconductor manufacturer with tremendous fab capacity for its advanced microprocessors. As process technology improves, however, CPU production moves to the latest fabs, freeing capacity in older processes. Using this capacity for chip sets and graphics controllers can maximize the return on its fab investment. In addition, high-performance system logic and graphics accelerators can spur demand for Intel's more profitable CPU products.

In the past few years, Intel has become the leading vendor of both system-logic chip sets and motherboards for PCs. It would not be surprising to see Intel become the top seller of graphics chips three years from now. Even if this change occurs, there will still be plenty of room for other vendors in the market, particularly if Intel chooses to focus on leading-edge 3D performance. But with too many vendors already in this market, some consolidation is inevitable.

Vendors Clash on Low-Cost Computers

Game Machines, Network Computers, Low-End PCs Attack $500 Price Point

by Linley Gwennap

PC TECH FORUM

It is a simple rule of economics: cutting the price of an item increases demand for it. But when PC vendors have tried selling systems at prices below $1,000, these units offered unsatisfying performance and did not sell well. With interest in the Internet and the World Wide Web now growing, several companies are making another run at this potentially large market for low-cost computers, this time using a network paradigm.

At the recent PC Tech Forum (PCTF), several vendors explained or, better yet, demonstrated their plans for this market. Acorn and Sun showed prototypes of their network computers based on ARM and SPARC processors, respectively. Diba discussed its software for "information appliances," and Sega explained how its new Saturn game player can be used to roam the Internet. The standard PC architecture, perhaps with a few modifications, could also be used at low price points.

A Market Opportunity for Low-Cost Systems

With an average price tag of about $2,000, the home PC has appealed mainly to users with an annual income of at least $40,000. This group also tends to be college-educated and thus better able to deal with the complexities of today's PCs. But in the U.S., 57% of these high-income households now own a PC, dampening sales growth. (In Europe and other areas, this income group is less saturated.)

A new low-cost computer could generate significant growth by attracting more buyers in the $20,000–$40,000 income range, where penetration is currently low. Addressing this market requires more than just low prices, however. Many of these buyers have less education and more unease about computers than those who own PCs today. A significant improvement in ease of use is needed to attract these potential buyers.

To create a complete value proposition, some desirable applications are needed. For many current PC buyers, a key purchase driver is the need to take work home. For people who don't use computers at work (or don't bring work home) the applications that encourage a computer purchase are (roughly in priority order) games, educational programs, and access to the Internet. Today, the most popular computing device in these middle-income households is a Nintendo or Sega game machine.

A corresponding opportunity exists in businesses. In a corporation, the purchase cost of a PC is less than the training and support cost required to keep that PC operating effectively. Computers that are much easier to use and maintain could save businesses huge amounts of money. For many corporate users, the key applications are e-mail, remote data access, and basic word processing, for which a low-cost system could provide adequate performance.

The Network Computer: Simplifying PCs

A group of vendors, of which Oracle has been the loudest, is promoting the concept of a network computer (NC). Although many have focused on the NC's potential $500 price tag, the key aspect of the NC is its lack of local storage—most programs and user data are stored remotely. If user-managed local storage is eliminated, all system maintenance can be performed remotely, greatly reducing the cost of maintenance and, at least from the user's point of view, making the NC easier to use than a PC.

This change in paradigm means that Windows 95 cannot be used as the NC operating system; the Microsoft OS assumes it is running from a local hard disk. Microsoft could create a product to address this new concept, but the software giant has so far shown little interest in the NC. This

Figure 1. At the PC Tech Forum, a number of industry representatives discussed low-cost computers, including (from left) Jim Louderback (*Windows Sources*), Joe Miller (Sega Soft), Steven McGeady (Intel), Mark Moore (Diba), Prabhat Mishra (Sun), Malcolm Bird (Acorn), and moderator Michael Slater (MDR).

leaves an opening for other software vendors; Oracle, the world's second largest, and Sun have stepped to the fore.

Oracle is developing a simple NC operating system as well as server software that would work with its popular database applications. Sun is building a Java-based OS for the client side. Both companies would benefit greatly from the increased sale of the servers required to support a large base of NCs as well as from client licensing fees.

From the hardware standpoint, the cost of an NC can be reduced by including less memory than in a PC, as the NC operating system would presumably be less complex than Windows 95. The vendors hope to further reduce cost by using an inexpensive non-Intel processor such as an ARM or, in Sun's case, a Java processor. With no local hard drive and, in some environments, a television instead of a monitor, an NC could be sold for $500 or less.

The drawback to eliminating the local hard disk is performance: application code and user data must be downloaded from the remote server through a relatively slow link. In a corporate environment, NCs could be connected to the server through a shared 10- or even 100-Mbps Ethernet link, providing reasonable performance if the network is not overloaded. A similar arrangement could be used in hotels, airports, and schools. For small businesses and particularly homes, however, the link would typically be through a 28.8-kbps modem or, at best, a 128-kbps ISDN line, limiting performance in many situations. If cable-modem service becomes widespread, these remote locations will eventually have access to higher bandwidth. In all these scenarios, users accustomed to hard-disk speeds may be disappointed.

Oracle, joined by Sun, IBM, Apple, and Netscape, recently announced the NC Reference Profile 1 (for a copy, see *www.nc.ihost.com*). While the specification is broad enough to encompass most PCs as well as any potential NC, it provides a framework for vendors to build clones of the Oracle NC as well as similar devices using different architectures. IBM, for example, said it will build an NC, based on its PowerPC 403 chip, for shipment by the end of the year; the unit, sans monitor, will sell for about $700.

Acorn Readies Platform for Oracle

Oracle, a software company, is relying on Acorn to develop the hardware for its ARM-based NC. Acorn Network Computing is a subsidiary of Acorn Computer, which made its name selling ARM-based PCs in the United Kingdom. The subsidiary was formed to adapt Acorn's set-top box, which is already going through trials in the U.K., for Oracle's use. As PCTF moderator Michael Slater noted, Acorn provides the hardware and "Oracle provides the hype."

Starting with a known platform accelerated Acorn's NC efforts. The initial version uses the highly integrated ARM 7500 processor (see MPR 11/14/94, p. 24), which contains audio, video, and I/O interfaces along with an ARM7 CPU. It contains no hard drive, no CD-ROM drive, and only 4M of ROM for the boot code, operating system, and Web browser, obtaining all other information from the server. (Some versions may contain other small applications in ROM.)

For home use, the system can directly drive an NTSC or PAL television and uses a 28.8-kbps modem to connect to the server. It can also be configured for business environments with an Ethernet adapter, connecting to a monitor instead of a TV. Both Oracle and Acorn say initial systems will begin shipping in September of this year from Acorn and other unnamed vendors.

At PCTF, Acorn's Malcolm Bird demonstrated a prototype unit downloading Web content and displaying it on an NTSC television. Bird noted the company had added anti-aliasing and other technology to obtain the appearance of a VGA monitor from a relatively low resolution TV screen. Indeed, the images seemed fairly sharp. The demonstration also included other basic tasks such as word processing, video, and audio playback.

For More Information

Contact Acorn Computer Group (Cambridge, England) at 44(0).1223.518518; fax 44(0).1223.518520 or send e-mail to *info@om.acorn.co.uk*.

Contact Cirrus (Fremont, Calif.) at 510.226.2373; fax 510.226.2070 or access the Web at *www.cirrus.com*.

Contact Oracle Corporation (Redwood City, Calif.) at 415.506.7000; fax 415.506.7132 or access the Web at *www.oracle.com*.

Contact Dhaval Ajmera at Sun (Sunnyvale, Calif.) at 408.774.8660; fax 408.774.8769.

Contact Diba (Belmont, Calif.) at 415.596.1177; fax 415.596.1188 or access the Web at *www.diba.com*.

Contact Sega (Redwood City, Calif.) at 415.802.6340 or access the Web at *www.sega.com*.

Cirrus Targets NC with ARM 7500FE

A subsequent version of the Acorn NC will be built around the recently announced ARM 7500FE. This device, specified by Acorn and designed by ARM, is similar to the 7500 but adds support for EDO DRAM and hardware floating point. Cirrus Logic will fabricate and market the 7500FE.

The 7500FE is the first ARM chip to contain a floating-point unit. The double-precision FPU was designed by ARM years ago but shelved due to lack of interest. Acorn revived the FPU for the 7500FE, hoping to perform signal-processing tasks on the host CPU. A 20% speed boost from the original 7500, to 40 MHz, should also help performance. Cirrus expects to sample the 7500FE in 3Q96, with shipments by year end. The company has not yet announced a price for the new device; for comparison, the 7500 now sells for $24.

Acorn is also working on a StrongArm version of the NC and hopes to have prototypes complete this year. The StrongArm processor (see MPR 11/13/95, p. 16) offers six

Component	Cost
Java CPU	$50
4M DRAM	$80
3M Flash	$40
PCI Video	$70
Audio	$30
Ethernet	$60
Super I/O	$10
Misc. Logic	$50
PCB	$20
Enclosure	$20
Power Supply	$15
Total Cost	**$445**

Table 1. Sun's proposed Java-based NC totals $445 in materials cost. (Source: Sun)

times the performance of the ARM 7500, but current versions have none of the 7500's peripherals. The extra performance could speed signal processing, eliminating the need for some peripherals, and could improve the performance of the user interface and other software.

Sun Serves Up Java NC

As one might expect, Sun sees the main purpose of the NC as executing Java. In this scenario, NC users would do little other than surf the Web and perform simple tasks (e.g., word processing, e-mail, spreadsheets) using downloaded Java applets. Sun is counting on the availability of a wide variety of applets to handle these day-to-day tasks. Thus, while the Acorn NC supports Java, the Sun NC is awash in it.

Sun has little experience with the consumer market and at this time is mainly targeting its current corporate customers. Sun originally called its device the zero-administration client (ZAC), emphasizing the reduced support and maintenance costs for its system.

At PCTF, Sun's Prabhat Mishra demonstrated an NC prototype, this one based on a MicroSparc-2 CPU. Running a beta version of JavaOS, Sun's standalone Java environment, the system was able to display Web content. Based on the demonstration, however, the software did not appear as fully developed as Acorn's.

Sun expects to ship a system based on the lower-cost MicroSparc-2ep processor (see MPR 5/6/96, p. 5) by year end. Over time, Sun expects to reduce costs further by switching to one of its forthcoming Java processors (see MPR 2/12/96, p. 4). Mishra presented a potential bill of materials, shown in Table 1, that totals $445 for this system. Although this cost leaves very little margin at a potential $500 price tag, the estimates in the table are quite conservative; we believe this system could easily be built for less than $300 in 1997.

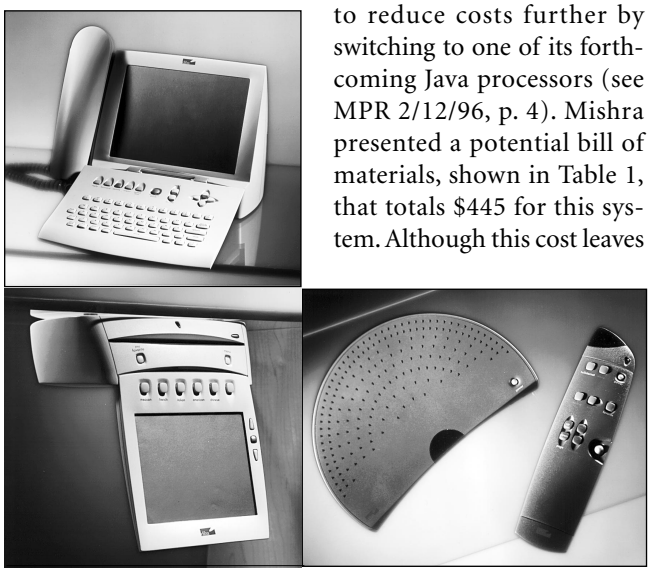


Figure 2. Diba's product ideas include (top) the Diba E-mail, (bottom from left) the Diba Kitchen, and the Diba Internet.

Diba Partners with Zenith

Farzad Dibachi, who founded Diba last year along with brother Farid, was a senior vice president at Oracle's New Media Division and so is well acquainted with the NC. Diba is taking the NC concept a step further, promoting single-function information appliances so easy to use they no longer appear to be computers. The startup has developed a software environment for these low-cost systems.

This software, which Diba calls its application foundation, is only about 300K in binary form but contains a real-time multitasking operating system, error handling, memory management, and standard graphics and I/O drivers suitable for these simple appliances. Diba has defined an API for applications to access the graphics and I/O in a hardware-independent fashion. The entire environment is CPU independent, although the initial development was done on a Motorola 68000-family processor.

Information appliances are targeted mainly at home users. Diba has lots of product ideas for the kitchen, for a set-top box, for e-mail access, for shopping, for schools, and other applications. It has even commissioned some provocative case designs, shown in Figure 2, created by the design firm Pentagram. Diba itself is not in the business of selling these devices; its role is to license its software and product ideas to other vendors that will build and market them.

The first vendor to take such a license is Zenith, which plans to incorporate Diba's software into a line of Internet-ready "NetVision" TV sets. These large-screen TVs will be coupled with a device similar to the Internet unit in Figure 2. Zenith expects the combination to sell in retail outlets by the end of this year starting at less than $1,000. Diba expects to soon sign several large Asian consumer-products vendors to build and market some of its other product ideas.

Diba has a clear focus on providing a simple interface to the user. At PCTF, Diba's Mark Moore repeated the company mantra: "the plastic is the application." In other words, each Diba system has a single target application (recipe book, e-mail, Web access, etc.), and the controls for that application are built into the plastic case. Operation of the device should be intuitive from the shape and design of the case; the user need not wade through complicated cascading menus to complete a task.

This focus on simplicity is needed in the consumer market. Diba must, however, find a compelling combination of price and features for its devices to succeed. The Web browser, for example, is only as compelling as the Web itself, which is still fairly daunting to the average consumer. The Kitchen system combines a CD player, a TV tuner, and a virtual cornucopia of recipes. With its licensing strategy, Diba can generate many ideas at a low cost, hoping to find at least one successful product.

Sega Offers Hot Games, Web Access

Sega may have the best near-term approach for home systems. The company is offering its Saturn game machine and a 28.8-kbps modem for $398. Saturn is built around three Hitachi SH processors and includes a CD-ROM drive, unlike the proposed NCs. The Saturn alone lists for $199, so consumers who already want a high-end game machine with lots of existing software can get on the Internet for an incremental cost of just $199, far less than the price of any NC.

Sega offers a dial-in service with unlimited connect time for $19 per month. The focus of this service is, predictably, game tips, multiplayer games, and tournaments, but the service includes Internet and Web access.

The economies of scale of its Saturn system allow Sega to offer its hardware at rock-bottom prices. The traditional model in the game market is to sell the hardware at cost, making profits solely on the software. This model could make it difficult for NC makers to compete with Sega for home users who just want to play games and surf the Web.

Another advantage of the Saturn system is its CD-ROM player. Although the system has the same bandwidth limitations as any diskless home unit running off a modem, users can load applications and other data from CD-ROMs much faster than in an NC. Saturn users could obtain large quantities of data by ordering a CD-ROM through the mail with a potentially higher bandwidth than by downloading such data across a telephone line.

Low-Cost PCs Could Also Fit the Bill

None of the aforementioned platforms offers compatibility with popular PC applications. At PCTF, MDR analyst Yong Yao presented a bill of materials, shown in Table 2, for a Pentium-166 system with no hard drive or monitor. He estimates such a device could be built in 2H97 for $290, easily supporting a $400–$500 retail price. This system would use the same client/server paradigm as the NC, keeping applications and user data on a remote server, but it would provide compatibility with full-fledged PCs. Thus, it could be used for working at home as well as for games, e-mail, Web access, and a wide variety of other applications. It could also be used in schools, hotels, and corporations.

A key enabler for this type of device, which Yao dubs the media computer, is for Microsoft to develop a "lighter" version of Windows 95 that is able to run directly from ROM. Keeping the operating system in ROM reduces the amount of DRAM needed and also avoids configuration errors. The new OS must also be much easier to use than the current Windows 95. Such a product could be derived from Microsoft's Pegasus project, an OS being developed for handheld computers, but Microsoft has not acknowledged any developments for an OS aimed at new low-cost systems.

Apple is taking a hybrid approach. Its Pippin platform, now marketed as the @World by Bandai at $599, is essentially a stripped-down Macintosh, with a CD-ROM drive but no hard disk, that uses a television as the display. Mac software can easily be modified to run on Pippin, and once modified, the new software can support both platforms. This similarity should jump-start the software market for Pippin and make it easy for users to share applications and data between the two platforms. Microsoft could take a similar approach and build an OS for low-cost x86 systems that offers some, but not full, PC compatibility.

Component	Cost
Pentium-166-class CPU with MMX	$100
8M SDRAM	$50
4M ROM + MC operating system	$35
Core logic + video for USB and 1394	$25
2D/3D + video + 2M frame buffer	$30
Case, power supply, and other	$50
Total in 2H97	**$290**

Table 2. In 2H97, a diskless "media computer" using a Pentium-166 could cost as little as $360 to build. (Source: MDR)

There are significant issues for any of these client/server designs. In addition to the bandwidth problem, some users are concerned about the privacy and security of data kept on a remote server. At PCTF, Intel's Steven McGeady noted the monthly cost of supplying the client with the necessary applications and remote data storage has not been defined. NC backers assume this service can be bundled with the standard $19/month Internet access fee with little or no extra cost, making a diskless system attractive.

If there is a significant premium, however, this extra monthly cost would rapidly surpass the cost of a hard drive. In a corporate environment, this extra cost would appear in the form of large new server systems required to support the diskless clients; from this standpoint, the client/server architecture simply shifts costs from the client to the server. Other panelists pointed out, however, the goal is not so much to reduce hardware costs as it is to reduce support costs; the client/server approach is critical in this regard.

Birth of a New Platform

The NC backers hope they are presiding over nothing less than the birth of a new platform. With the first products already shipping and others expected this year, these vendors have more than vaporware, but it is too early to tell which approaches will succeed and whether any will approach the PC in popularity. For home use, an important enabler will be the inexpensive delivery of high-bandwidth infrastructure: ADSL, cable modems, or some other method.

The market needs being addressed—low cost and ease of use—could be handled by systems based on reduced-cost versions of Intel processors and Microsoft operating systems. Yet these two vendors, particularly Intel, don't seem interested in low-cost products, letting upstarts like Oracle and Sun drive this emerging market. If the NC market grows as these vendors hope, they could establish a new axis to rival the Intel-Microsoft duopoly. But there is still plenty of time for the PC giants to make their mark in the NC world. M

LITERATURE WATCH

BUSES

CardBus configuration: a two-step process. A CardBus card combines the low power, small form factor, and light weight of a PC Card with the performance of PCI. However, proper configuration is essential to gain the full benefits of this device. Tom Shanley, Mindshare; *EDN,* 5/9/96, p. 111, 6 pp.

DEVELOPMENT TOOLS

Putting your money on Windows-based tools. Windows-based EDA tool development has boomed since the introduction of Windows 95. Jim Lipman, *EDN,* 5/23/96, p. 51, 7 pp.

DSPS

Avoiding DSP performance problems up front. This second half of a two-part article discusses optimal use of digital filters and A/D converters in DSP system design. Gene Pikus, Alliant Techsystems; *Electronic Design,* 5/13/96, p. 83, 7 pp.

New vocoder modeling doubles recording time. TI's MSP58C83x handles voice compression in a digital telephone answering machine. Paul McGoldrick, *Electronic Design,* 5/13/96, p. 139, 3 pp.

GRAPHICS/VIDEO

Multimedia decoder chip adds a hot "SPARC" to DVD. DVD applications will enjoy added performance and flexibility, thanks to a single-chip decoder that packs an embedded MicroSparc processor. Peter Fletcher, *Electronic Design,* 5/13/96, p. 59, 5 pp.

Frame-buffer wars: new directions in PC graphics. The battle between the dedicated frame buffer and the UMA is a skirmish in the old war between available bandwidth and bandwidth consumption and between cost and performance. David Kocsis, Oak Technology; *EDN,* 5/23/96, p. 121, 5 pp.

MEMORY

Content-addressable memories add processing power to embedded systems. CAMs enable you to apply associative processing to designs that require list searches and data translation. Tom Weldon, Music Semiconductors; *EDN,* 5/9/96, p. 137, 10 pp.

MISCELLANEOUS

Java: virtual machine for virtually any platform. Java appears attractive for embedded applications but needs enhancements for any real-time work. Simon Waddington, Stephan Li, Wind River; *Embedded Systems Programming,* 6/96, p. 27, 10 pp.

Digital TV: please stand by. Outfitting today's terrestrial broadcast networks for digital will be a costly undertaking, to say nothing of the many political battles that still lie ahead. George Leopold, *OEM Magazine,* 5/96, p. 24, 9 pp.

The interview: Bill Gates. Gates shares his views on Microsoft's push toward the consumer PC, a revived PDA program, the on-again relationship with Intel, and the bandwidth problem. Rick Boyd-Merritt, *OEM Magazine,* 5/96, p. 37, 6 pp.

A balancing act in displays. For designers of handheld systems, the display picture has been either a dim or a costly one, but that scenario could change with some new flat-panels on the horizon. David Lieberman, *OEM Magazine,* 5/96, p. 62, 9 pp.

PROCESSORS

Multimedia instructions boost host-based processing. Multimedia instructions capitalize on a CPU's capability to perform parallel processing. Markus Levy, *EDN,* 5/23/96, p. 67, 9 pp.

The new 8051s. Intel's venerable 8051 has been updated over the years and has more recently inspired a variety of derivatives. Jan surveys the current field of 8051s and derivatives from Intel, Dallas, and Philips. Jan Axelson, Intel; *MicroComputer Journal,* 6–7/96, p. 9, 8 pp.

Using the 68HC11 SPI. The 68HC11 Serial Peripheral Interface allows data exchange rates of 1 Mbps using as few as three wires. Karl explains this little-understood but powerful subsystem at the register level. Karl Lunt, *MicroComputer Journal,* 6–7/96, p. 42, 6 pp.

SYSTEM DESIGN

Mixed-signal designs complicate debugging. Increasing use of both analog and digital signals on the same board is causing probing and crosstalk problems. John Novellino, *Electronic Design,* 5/13/96, p. 46, 5 pp.

Low-dropout regulators get application specific. Offspring of the ubiquitous three-pin linear regulators now target microprocessors and cellular telephones. Frank Goodenough, *Electronic Design,* 5/13/96, p. 65, 10 pp.

DSP software helps build a speakerphone. A full-duplex speakerphone can be designed using a 56002 DSP and PC Media technology. John Lane, Dan Hoory, et al, Motorola; *Electronic Design,* 5/28/96, p. 110, 6 pp.

Low-power system design: selecting the right μP. Guidelines for choosing a low-power CPU. J.S. Holmes, Boehringer Mannheim Corp.; *Electronic Design,* 5/28/96, p. 87, 4 pp.

Environmentally hardened PCs: how much is enough? Getting industrial PCs to measure up to all the standards required in embedded and industrial environments is a two-part problem. The first is to identify the conditions it has to meet, and the second is to make sure the technology is available. Warren Andrews, *RTC,* 5/96, p. 77, 2 pp.

RECENT IC ANNOUNCEMENTS

PART NUMBER	VENDOR	DESCRIPTION	PRICE/QUANTITY	AVAILABILITY
MICROPROCESSOR				
88C166-5M	Siemens 408.777.4500	16-bit microcontroller operates at 20 MHz and includes 32K of flash memory accessible via internal 32-bit bus for improved performance.	$37/1,000	Prod.—Now
W65C02S	WDC 602.962.4545	Venerable 6502 microprocessor moves to 0.8-micron process, boosting speed to 16 MHz and allowing 3.3-V operation; also integrated versions.	$2/100,000	Prod.—Now
INTERFACE				
PCT288I	PC-Tel 408.383.0452	Modem chip supports data rates of 33.6 kbps and fax at 14.4 kbps using data processing from Pentium host; with 8-/16-bit ISA interface.	$35/10,000	Prod.—Now
SC82C168	Philips 408.991.3626	Media-access controller (MAC) handles 10/100-Mbps Ethernet with few external components; includes PCI interface, 10BASE-T transceiver.	$23/50,000	Prod.—Now
MEMORY				
M29V040	SGS-Thomson 617.259.0300	Flash memory has 4-Mbit capacity, organized as 512K×8, and runs from a single 3.3-V supply with 120-ns read-access time; in PLCC and TSOP.	$11.50/11,000	Prod.—Now
M27C405	SGS-Thomson 617.259.0300	One-time programmable (OTP) PROM has 4-Mbit capacity (512K×8), 70-ns access time, 5-V read voltage, 12.75-V program voltage.	$6.90/11,000	Prod.—Now
2480A	Music Semi 719.570.1550	Content-addressable memory (CAM) has 2K×64 capacity, provides data-efficient searching for LAN equipment; in 70-, 90-, and 120-ns speeds.	$38/1,000	Prod.—Now
MT41LC256K32D4	Micron 208.368.4400	Synchronous graphics DRAM (SGRAM) has 8-Mbit capacity, organized as 256K×32, runs at 66 MHz from 3.3-V supply; in TQFP-100 package.	$30/10	Samples—Now Prod.—3Q96
Am29F800	AMD 408.749.5703	Flash memory has 8-Mbit capacity, configurable as 512K×8 or 256K×16, and operates from a single 5-V supply; guaranteed for 100,000 cycles.	$23.10/1,000	Prod.—Now
MISCELLANEOUS				
ST5090	SGS-Thomson 617.259.0300	Voice coder/decoder for portable communications applications operates from single 3.3-V supply and consumes only 21 mW in operation.	$4.96/10,000	Prod.—Now
EZ117 ES117A	Semtech 805.498.2111	Low-dropout voltage regulators provide 3.3-V DC supply from 5-V source; with 800-mA (117) or 1-A (117A) source current and 1.2-V dropout.	$1.45/200	Prod.—Now
LX5285	Linfinity 714.898.8121	Voltage regulator provides 800-mA source, 400-mA sink fixed 2.85-V voltage source for SCSI systems and peripherals; in SOT-223 package.	$2.45/1,000	Samples—Now Prod.—3Q96
PROGRAMMABLE LOGIC				
ATF16V8C-5	Atmel 408.441.0311	PLD is flash based and offers 5-ns worst-case pin-to-pin delay and 90-mA operating current draw; in dual-inline and surface-mount packages.	$7.14/100	Prod.—Now
SYSTEM LOGIC				
PSD304R	WSI 510.656.5400	Microcontroller peripheral includes 256K of program store, I/O pins, and programmable logic; interfaces to most 8-bit microcontrollers; in TQFP-44.	$8.22/5,000	Prod.—Now

PATENT WATCH

by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send comments or questions via e-mail to belgard@umunhum.stanford.edu.

5,491,829

Method and system for indexing the assignment of intermediate storage buffers in a superscalar processor system
February 13, 1996
Inventors: Chin-Cheng Kau, et al
Assignee: IBM
Filed: May 11, 1995
Claims: 6
A method and system for instruction dispatch efficiency in a superscalar processor system having multiple intermediate storage buffers, multiple general-purpose registers, and a storage-buffer index. Each of the scalar instructions generally includes at least one source and one destination. One buffer is assigned to the destination of a scalar instruction. A relationship between that buffer and a GPR is stored in the buffer index. A result from the scalar instruction is stored in the chosen buffer when the instruction is executed. The index is used to determine which buffers to use as source operands for subsequent instructions until the GPR is updated.

5,491,353

Configurable cellular array
Issued: February 13, 1996
Inventor: Thomas A. Kean
Assignee: Xilinx
Filed: March 31, 1995
Claims: 9
A configurable cellular array is provided having a two-dimensional array of cells in which each cell in the array has at least one input and output connection at least one bit wide to its neighbors. Each cell also has a programmable routing circuit to permit intercellular connections to be made. In one arrangement, each cell contains a programmable function unit that includes multiple multiplexers. The function unit and routing unit are programmable using associated random access memory (RAM) areas within the cell. Each cell may be coupled to at least one global or array-crossing signals so all cells can be signaled simultaneously.

5,490,280

Apparatus and method for entry allocation for a resource buffer
Issued: February 6, 1996
Inventors: Shantanu R. Gupta, et al
Assignee: Intel
Filed: June 28, 1994
Claims: 44
A method and apparatus for allocating vacant entries of a buffer resource and generating a set of enable vectors for a set of issued instructions. A deallocation vector of a reservation station is searched to locate, within one clock cycle, the vacancies within the reservation station for operands of several issued operations. Vacancies are indicated by bits of the deallocation vector. General static and dynamic approaches are disclosed for performing the vacant entry identification at high speed within a single clock cycle.

5,490,265

Late cancel method and apparatus for a high-performance microprocessor system
Issued: February 6, 1996
Inventors: Robert M. Riches, Jr., et al
Assignee: Intel
Filed: April 14, 1993
Claims: 18
A late cancel method and apparatus used in a microprocessor system consisting of a processor, an external cache memory, and a main memory. An instruction request by the processor to the external cache is presumed to have hit in the cache. The instruction is predecoded and decoded in parallel with determining whether or not the external cache hit. If the external cache hit, the instruction is processed; if the external cache missed, the instruction is aborted and a main-memory access is made to obtain the instruction.

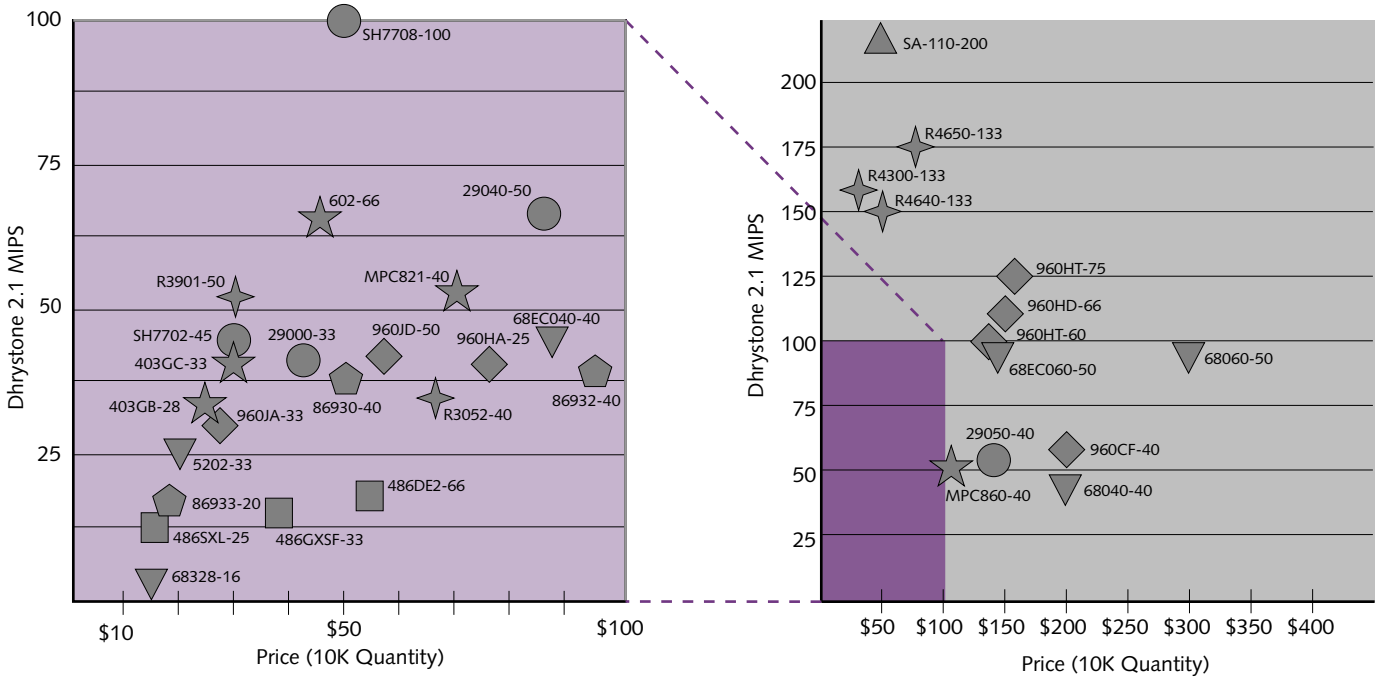
5,490,059

Heuristic clock-speed optimizing mechanism and computer system employing the same
Issued: February 6, 1996
Inventors: Rupaka Mahalingaiah, et al
Assignee: AMD
Filed: September 2, 1994
Claims: 13
A microprocessor includes a programmable thermal sensor incorporated on an associated die for generating a temperature signal. The signal is provided to a frequency synthesizer that controls the frequency of the CPU clock signal. The frequency synthesizer is dynamically controlled such that the frequency of the CPU clock signal is varied to run at an optimal frequency while preventing the microprocessor from overheating.

OTHER ISSUED PATENTS

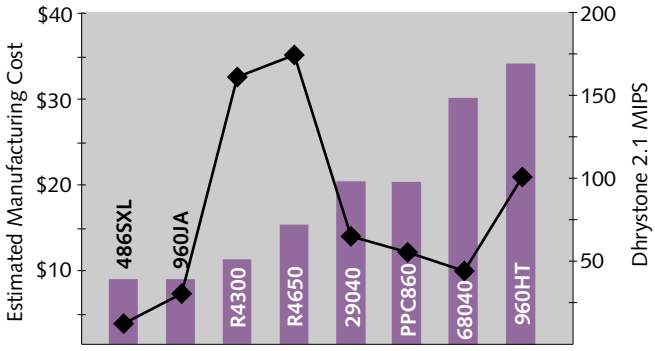
5,490,255 *Expedited execution of pipelined command having self-ordering operand processing requirements*
5,493,660 *Software-assisted hardware TLB miss handler*
5,493,659 *Data processor providing fast break in program execution* M

CHART WATCH: EMBEDDED PROCESSORS



This Chart Watch covers 32-bit and 64-bit embedded microprocessors. The table below and the chart at the upper right show the price/performance positions for a number of embedded CPUs; the chart above is an inset for the lowest priced of these processors.

The chart on the right compares integer performance (diamonds) and estimated manufacturing costs (bars) for a number of embedded microprocessors according to the MDR Cost Model.



	NEC R4300	IDT R4650	Intel 486GXSF	Intel 960JA	Intel 960HT	Motorola 68EC040	Motorola 68EC060	AMD 29040	Motorola 860DC
Architecture	MIPS	MIPS	x86	i960	i960	68K	68K	29K	PowerPC
Clock rate	133 MHz	133 MHz	33 MHz	33 MHz	60 MHz	40 MHz	50 MHz	50 MHz	40 MHz
I/D cache	16K/8K	8K/8K	8K	2K/1K	16K/8K	4K/4K	8K/8K	8K/4K	4K/4K
FPU?	Yes	Yes	No	No	No	Yes	Yes	No	No
MMU?	Yes	Yes	Yes	No	No	Yes	Yes	Yes	Yes
Bus width	32 bits	64 bits	16 bits	32 bits	32 bits	32 bits	32 bits	32 bits	32 bits
Bus frequency	66 MHz	66 MHz	33 MHz	33 MHz	20 MHz	40 MHz	25 MHz	25 MHz	40 MHz
MIPS	160 MIPS*	175 MIPS	15 MIPS*	28 MIPS	100 MIPS*	44 MIPS	90 MIPS	67 MIPS	52 MIPS
Voltage	3.3 V	3.3 V	2.7/3.3 V	3.3 V	3.3 V	5 V	3.3 V	3.3 V	3.3 V
Power (typ)	2.2 W	3.8 W	0.5 W	0.5 W	4.5 W	4.5 W	n/a	1.7 W	0.9 W
MIPS/watt	73	46	29	56	22	10	n/a	39	58
MIPS/$ (price)	5.00	2.46	0.38	1.00	0.73	0.50	0.63	0.78	0.51
Transistors	1,700,000	1,050,000	n/a	750,000	2,300,000	1,170,000	2,530,000	1,200,000	1,800,000
IC process	0.35µ 3M	0.6µ 3M	0.8µ 2M	0.8µ 3M	0.6µ 4M	0.65µ 3M	0.5µ 3M	0.7µ 3M	0.5µ 3M
Die size	45 mm²	56 mm²	n/a	64 mm²	100 mm²	163 mm²	217 mm²	119 mm²	25 mm²
Est mfg cost*	$11	$15	$15	$8	$34	$30	$75	$20	$20
Availability	2Q96	Now	Now	Now	2Q96	Now	Now	Now	Now
Price (10K)	$32	$71	$40†	$28	$137	$88	$142	$86	$102

n/a: information not available † list price in 1,000s (Source: vendors except *MDR estimates)

The ABCs of DSPs

DSP stalwart Berkeley Design Technology (BDT) has released a guide to DSP basics geared toward engineers and engineering managers. ***DSP Processor Fundamentals****: Architectures and Features* fills its 220 pages with introductory material on numerical formats, data paths, instruction sets, execution control, and pipelining.

Initial copies of the book list for $60, with discounts available for volume purchases. For more information, or to order, call BDT (Fremont, Calif.) at 408.997.1842; fax 408.268.5623; or send e-mail to *info@bdti.com*.

Benchmarks for Batteries from BAPCo

The Business Applications Performance Corporation (BAPCo) has developed the **SYSmark for Battery Life** benchmark suite to measure and compare battery life in PC-compatible notebook computers. The scripted benchmarks run commercial business productivity applications the way a user might actually run them, including idle periods between applications.

The benchmark package, which costs $995, is delivered on CD-ROM and includes a photocell for monitoring the intensity of the computer's screen and a mechanical actuator for pressing keys on the keyboard. For more information, contact BAPCo (Santa Clara, Calif.) at 408.988.7654; fax 408.765.4920; or visit *www.bapco.com*.

Best PC Prices in Town!

The ***PC Street Price Index*** is a monthly newsletter published by Metro Computing that, as its name might imply, collates and lists the lowest street prices for several hundred different PC and Macintosh systems, hardware upgrades, peripherals, and software. Prices are collected from more than 1,500 retail, mail-order, catalog, and warehouse stores across the United States, and they are updated monthly.

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$100 Off a Stanford Education

Stanford University's Western Institute of Computer Science is holding its summer 1996 program in computer science from July through August. Week-long classes include such topics as Internet security, advanced Java, object data management, electronic commerce, code optimizations, electronic commerce, C++, and video.

Registration 14 days in advance of the class costs $1,450; regular tuition is $1,575. A $100 discount is available for multiple enrollments or for referring another attendee. For more information, contact WICS (Magalia, Calif.) at 916.873.0575; fax 916.873.6697; or visit *www-wics.stanford.edu/WICS.html*.