401GF Is Coolest, Cheapest PowerPC

IBM's Low-Power Processor Delivers 650 MIPS/Watt with a $13 Price Tag

by Jim Turley

For the first time, PowerPC chips can mount a credible assault on the market for low-cost battery-operated devices. Fulfilling a year-old promise, IBM Microelectronics rolled out its PowerPC 401 core, providing a new low end to the PowerPC family. The small new design maintains software compatibility with the range of PowerPC processors from IBM and Motorola but drops prices below $15.

At 25 MHz, the part merely sips power, consuming just 40 mW (typical) from a 2.5-V supply—one-fifth the power of previous embedded PowerPC chips and well into the target range for portable devices.

The 401 core is available both as a macrocell for ASIC development and as a packaged part, the 401GF. At $13 in quantity, the 401GF is the least expensive PowerPC chip made, yet it delivers 52.5 Dhrystone MIPS at 50 MHz. The 25-MHz and 50-MHz versions of the 401GF will begin sampling in a few weeks; 75- and 100-MHz versions will follow before the end of 1996, according to IBM.

Stripped to the Core

The 401GF achieves its remarkably low power consumption through a combination of design tradeoffs, circuit-design techniques, and fabrication process. As IBM's entry-level PowerPC, the 401 core includes only the features absolutely necessary for PowerPC compatibility. For example, the 401GF does not include the serial ports, MMU, DRAM controller, or DMA logic of the earlier 403-series parts *(see* **080601.PDF** *)*. As Table 1 shows, the 401GF includes little more than a 401 core, dual caches, and a multiplexed bus interface.

By its nature as a PowerPC implementation, the 401GF has a somewhat richer feature set than most minimal embedded CPUs. For example, the chip supports simple static branch prediction, handles unaligned loads and stores, offers selectable byte ordering, includes a hardware multiply and divide unit, and has separate instruction and data caches. The 401's register file is triple ported, reducing pipeline stalls and contention for the internal buses.

The caches are more deluxe than usual for a low-cost chip. The data cache has a two-line write buffer, both caches can be locked on a line-by-line basis, and both forward the critical word first. In all, these features help the 401GF attain its 1.05 MIPS/MHz ratio. They also contribute to its relatively bulky die size.

Processor	401GF	403GA	403GB	403GC
Max freq	50 MHz	33 MHz	28 MHz	33 MHz
I/D cache	2K/1K	2K/1K	2K/1K	2K/1K
Dhry MIPS	52 MIPS	41 MIPS	35 MIPS	41 MIPS
Voltage	3.3 V	3.3 V	3.3 V	3.3 V
Power (typ)	140 mW	265 mW	200 mW	200 mW
Package	TQFP-80	PQFP-160	TQFP-128	PQFP-160
MMU?	No	No	No	Yes
DRAM ctrl?	No	Yes	Yes	Yes
DMA chan	None	4	2	4
Serial chan	None	1	1	1
Availability	2Q96	Now	Now	Now
Price (10K)	$13	$28	$25	$30

Table 1. The 401GF is similar to IBM's three 403-series parts in many respects, including the caches, but without the peripherals.

Optimized for ASICs

The first two versions of the 401GF, at 25 and 50 MHz, are fabricated in IBM's 0.5-micron three-layer-metal CMOS-5S process. At 4.5 mm^2, the 401 core is hardly oversize, but the inherent complexity of the PowerPC architecture does tip the scales a bit. The notoriously small ARM7 core, for instance, measures just 3.8 mm^2 in a less aggressive 0.7-micron process. LSI Logic's CW4001 covers 3.5 mm^2 in a comparable 0.5-micron process, less one metal layer. In IBM's favor, though, neither of these cores offers any of the performance features mentioned above.

IBM's design method is tailored for ASICs, even on its standard parts. Although not immediately clear from the die photo in Figure 1, the 401GF has two internal buses—one for low-latency units close to the CPU core and another for relatively long latency peripherals—with a bus bridge between them. Since the 401GF has no on-chip peripherals, the secondary bus sits unused; on its 403-series brethren, it hosts the serial channels. IBM is studiously building its library of peripheral functions, hoping to attract PowerPC-based ASIC customers that Motorola cannot service.

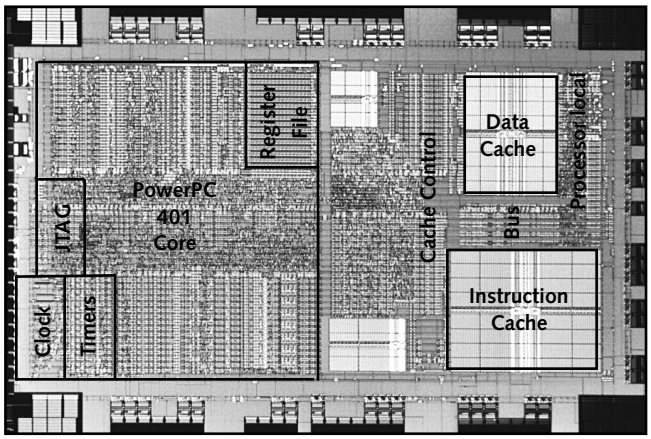

Figure 1. The 401GF is laid out for convenient ASIC development, so less than 25% (4.5 mm^2) of the chip's 22 mm^2 is dedicated to the PowerPC core in IBM's 0.5-micron three-layer-metal process.

Price & Availability

IBM's 401GF is sampling now in an 80-lead TQFP package; 75- and 100-MHz samples will be available near the end of 1996. In 10,000-piece quantities, the 401GF is priced at $13. For more information, contact IBM Microelectronics (Research Triangle Park, NC) via fax at 415.855.4121, or visit IBM's embedded PowerPC page at *www.chips.ibm.com/products/embedded/index.html*.

Conditional Clocking Quiets 401's Logic

The 401's three-stage pipeline is the minimum necessary for a contemporary RISC design, yet it allows the chip to reach competitive performance levels: IBM expects to sample the 75-MHz version before the end of the year and, with a possible process shrink to 0.35 micron, a 100-MHz chip. The ARM7 core, in contrast, is currently limited to 40 MHz without expanding its three-stage pipeline into five stages.

The 401GF relies heavily on conditional clocking and clock-distribution tricks. Individual sections of the 401 core are clocked only as necessary, with registers, execute stages, and buffers idled when not in use. The 401GF also has four user-selectable power-down states, from wait mode, which stops fetching and cuts power in half, to deep sleep, which halts all circuits while power consumption plummets to just 0.015 mW. Resuscitating the 401GF from deep sleep requires a hardware interrupt and a good 1.5 milliseconds, or 37,500 cycles at 25 MHz.

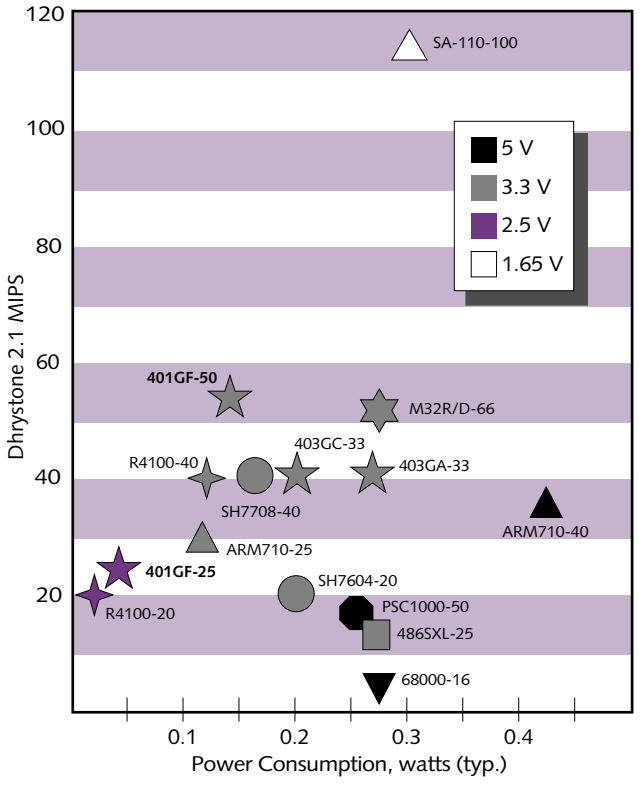

Figure 2. The 401GF's low power consumption compares favorably with that of a number of other recently announced embedded microprocessors. (Source: vendors)

Good for Low Power

The chip's estimated power consumption is impressively low. At 25 MHz, the 401GF draws about 16 mA from its 2.5-V supply, for 40 mW of typical power consumption. At 656 MIPS/watt, the 401GF unseats even the impressive StrongARM-110 *(see* **100201.PDF** *)* in power/performance efficiency, though it comes nowhere near the Digital chip's high-end performance. As Figure 2 shows, the 401GF comes in a close second behind NEC's 20-MHz R4100 *(see* **090403.PDF** *)*, which, at just 27 mW and 20 MIPS, stands out with an amazing 815 MIPS/watt.

The 401GF can operate up to 25 MHz at 2.5 V; after that, a 3.3-V supply is required. The higher supply voltage has the side effect of giving the chip compatibility with conventional 5-V I/O levels.

Turning up the clock frequency on the puny PowerPC increases performance linearly, but its power consumption climbs even faster because of the jump to 3.3 V. At 50 MHz, the 401GF needs closer to 140 mW, dropping its MIPS/watt ratio to about 375—still an efficient part. At 100 MHz, the 401GF will give the 100-MHz SA-110 a run for its money, coming within a few percent of Digital's estimated integer performance and power consumption—and all from a 3.3-V supply, twice the voltage of the SA-110 core.

The economic ratios are just as good. IBM is pricing both the 25-MHz and the 50-MHz versions of its new chip at $13 in 10,000-unit quantities. These prices are less than half that of the cheapest SA-110 and cheaper than the R4100's. The 401 challenges low-cost products like Hitachi's SH-3 family and NEC's V800 line. Unlike those architectures, PowerPC has a broad, clear upgrade path to higher performance and (at least in the midrange) an alternate vendor.

IBM Picking Up Speed in Embedded Market

IBM has come a long way since the company began its embedded PowerPC line two years ago. Although the chips in IBM's embedded line were sometimes hard to tell apart, the company is now beginning to grow into a full-line microprocessor supplier. For the next few years, IBM will continue to emphasize its core-based ASIC capabilities rather than its thin catalog of standard designs. The ASIC designs will fill the fabs and cover the time the company needs to assemble a credible array of standard peripherals.

For consumer-electronics and portable-communications-gear makers with the wherewithal for ASIC development and a taste for PowerPC, IBM is the obvious choice. But even without the "brand name" recognition of the world's best-selling desktop RISC processor, IBM has created a very competitive 32-bit embedded CPU that stacks up well against the best. M