PATENT WATCH

by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send comments or questions via e-mail to belgard@umunhum.stanford.edu.

5,491,829

Method and system for indexing the assignment of intermediate storage buffers in a superscalar processor system
February 13, 1996
Inventors: Chin-Cheng Kau, et al
Assignee: IBM
Filed: May 11, 1995
Claims: 6
A method and system for instruction dispatch efficiency in a superscalar processor system having multiple intermediate storage buffers, multiple general-purpose registers, and a storage-buffer index. Each of the scalar instructions generally includes at least one source and one destination. One buffer is assigned to the destination of a scalar instruction. A relationship between that buffer and a GPR is stored in the buffer index. A result from the scalar instruction is stored in the chosen buffer when the instruction is executed. The index is used to determine which buffers to use as source operands for subsequent instructions until the GPR is updated.

5,491,353

Configurable cellular array
Issued: February 13, 1996
Inventor: Thomas A. Kean
Assignee: Xilinx
Filed: March 31, 1995
Claims: 9
A configurable cellular array is provided having a two-dimensional array of cells in which each cell in the array has at least one input and output connection at least one bit wide to its neighbors. Each cell also has a programmable routing circuit to permit intercellular connections to be made. In one arrangement, each cell contains a programmable function unit that includes multiple multiplexers. The function unit and routing unit are programmable using associated random access memory (RAM) areas within the cell. Each cell may be coupled to at least one global or array-crossing signals so all cells can be signaled simultaneously.

5,490,280

Apparatus and method for entry allocation for a resource buffer
Issued: February 6, 1996
Inventors: Shantanu R. Gupta, et al
Assignee: Intel
Filed: June 28, 1994
Claims: 44
A method and apparatus for allocating vacant entries of a buffer resource and generating a set of enable vectors for a set of issued instructions. A deallocation vector of a reservation station is searched to locate, within one clock cycle, the vacancies within the reservation station for operands of several issued operations. Vacancies are indicated by bits of the deallocation vector. General static and dynamic approaches are disclosed for performing the vacant entry identification at high speed within a single clock cycle.

5,490,265

Late cancel method and apparatus for a high-performance microprocessor system
Issued: February 6, 1996
Inventors: Robert M. Riches, Jr., et al
Assignee: Intel
Filed: April 14, 1993
Claims: 18
A late cancel method and apparatus used in a microprocessor system consisting of a processor, an external cache memory, and a main memory. An instruction request by the processor to the external cache is presumed to have hit in the cache. The instruction is predecoded and decoded in parallel with determining whether or not the external cache hit. If the external cache hit, the instruction is processed; if the external cache missed, the instruction is aborted and a main-memory access is made to obtain the instruction.

5,490,059

Heuristic clock-speed optimizing mechanism and computer system employing the same
Issued: February 6, 1996
Inventors: Rupaka Mahalingaiah, et al
Assignee: AMD
Filed: September 2, 1994
Claims: 13
A microprocessor includes a programmable thermal sensor incorporated on an associated die for generating a temperature signal. The signal is provided to a frequency synthesizer that controls the frequency of the CPU clock signal. The frequency synthesizer is dynamically controlled such that the frequency of the CPU clock signal is varied to run at an optimal frequency while preventing the microprocessor from overheating.

OTHER ISSUED PATENTS

5,490,255 *Expedited execution of pipelined command having self-ordering operand processing requirements*
5,493,660 *Software-assisted hardware TLB miss handler*
5,493,659 *Data processor providing fast break in program execution* M