PATENT WATCH

by Rich Belgard, Contributing Editor

The following U.S. patents are key patents related to the development and history of the microprocessor. Please send comments or questions via e-mail to belgard@umunhum.stanford.edu.

3,821,715

Memory system for a multichip digital computer
Issued: June 28, 1974
Inventors: Marcian (Ted) Hoff, Jr., Stanley Mazor, Frederico Faggin
Assignee: Intel
Filed: January 22, 1973
Claims: 17
A general-purpose digital computer consisting of multiple MOS chips is described. One chip includes a central processing unit coupled by bidirectional lines to RAM and ROM. The ROM stores instructions and other data. Each chip is mounted on standard 16-pin dual in-line packages. Input and output information to the computer is read in through and read out from terminals on the memory chips.

4,074,351

Variable-function programmed calculator
Issued: February 14, 1978
Inventors: Gary W. Boone, Michael J. Cochran
Assignee: Texas Instruments
Filed: February 24, 1977 (Priority: July 19, 1971)
Claims: 20
A variable-function calculator with a fixed program memory in which a number of programs are stored. The calculator includes a program counter, an instruction register, control decoders, jump-condition circuits, a clock generator, a timing generator, and digit and flag mask decoders. Besides providing basic desktop-calculator functions, the memory may be programmed. One version of the invention can be fabricated as a monolithic integrated semiconductor system utilizing contemporary metal-insulator-semiconductor techniques.

4,300,192

Method and means for storing and accessing information in a shared-access multiprogrammed data-processing system
Issued: November 10, 1981
Inventors: John F. Coleur, Robert F. Montee
Assignee: Honeywell Information Systems
Filed: November 14, 1978 (Priority: April 18, 1974)
Claims: 5
A combination of segmentation and paging in a computer system is described. Segments are defined by segment descriptors, which include a base address and a limit. Segments are of variable size. Subsequent to a logical address calculation, the segment may be further subdivided into fixed-size pages that are mapped onto physical addresses.

4,363,091

Extended address, single- and multiple-bit microprocessor
Issued: December 7, 1982
Inventors: William Pohlman III, Bruce Ravenel, James McKevitt, Stephen Morse
Assignee: Intel
Filed: June 31, 1978
Claims: 26
A microprocessor including a memory unit and a processing unit. The processing unit includes relocation registers that are shifted left and added to an offset portion to produce an extended address whose bit width is greater than the bit width of the offset portion or the relocation register width. Also includes zero-extension/sign-extension of immediate byte operands to word operands, depending on instruction format.

4,942,516

Single-chip integrated-circuit computer architecture
Issued: July 17, 1990
Inventor: Gilbert P. Hyatt
Filed: June 17, 1988 (Priority: November 24, 1969)
Claims: 41
A microcomputer architecture is provided that facilitates a fully integrated-circuit computer on a single chip. The architecture includes use of ROM for program storage, a RAM or scratch-pad memory for alterable operand storage, and integrated-circuit logic. Additional architectural features include serial data communication, pulse-modulated communication, 8-bit instruction bytes, 16-bit operand words, and shared I/O channels.

4,972,338

Memory management for microprocessor system
Issued: November 20, 1990
Inventors: John H. Crawford, Paul S. Ries
Filed: April 19, 1988 (Priority: June 13, 1985)
Assignee: Intel
Claims: 7
A microprocessor architecture for an address translation unit that provides two levels of memory management is described. Segmentation registers and an associated segmentation table in main memory provide a first level of memory management that includes attribute bits used for segmentation protection, priority, etc. A second page-cache memory and an associated page directory and page table in main memory provide a second level of management with independent protection on a page level. Optional paging of segments is provided. M