LITERATURE WATCH

AUDIO/VIDEO

H.324 paves road for mainstream video telephony. A standard for videoconferencing over ordinary phone lines has gained acceptance; now, hardware/software implementation issues remain. Jeff Child, *Computer Design*, 1/97, p. 107, 3 pp.

Videoconferencing calls new nets. Now that standards for video over LANs and analog phone lines are set and product prices have come down, this could finally be the year videoconferencing starts to take off. Andrew W. Davis, *OEM*, 1/97, p. 60, 7 pp.

BUSES

Intelligent I/O architecture enables faster, more flexible systems. The I_2O split-driver model reduces the plethora of drivers required for hardware compatibility. Pauline Shulman, Wind River; *Electronic Design*, 1/20/97, p. 125, 5 pp.

Serial bus opens the door for sealed PCs. IEEE 1394 offers the speed required for next-generation PCs and consumer electronics. Gregory Urban, National Semiconductor; *Electronic Design*, 2/3/97, p. 136, 3 pp.

Pit stop for the PC. Firewire will rev up desktop performance. David Lieberman, *OEM*, 1/97, p. 68, 8 pp.

Fieldbus delivers digital benefits to industrial applications. Fieldbus, an all-digital two-way communication system that connects control systems to instrumentation, offers significant benefits compared to traditional analog methods. Mike Santori, National Instruments; *Personal Engineering*, 2/97, p. 44, 6 pp.

DEVELOPMENT TOOLS

Low-end oscilloscopes. Benchtop and handheld oscilloscopes for under $6,000 offer an inexpensive solution for today's testing applications. *Electronic Products*, 2/97, p. 25, 4 pp.

IC DESIGN

Technology 1997 analysis and forecast: solid state. New lithography techniques will push transistor gate lengths below 0.25 microns. Linda Geppert, *IEEE Spectrum*, 1/97, p. 55, 5 pp.

New parasitic-extraction tools needed for DSM flows. IC designers face new challenges as geometries migrate toward 0.25-µm design rules. Cheryl Ajluni, *Electronic Design*, 1/20/97, p. 111, 7 pp.

Complex ASICs straining verification resources. Chip designers can't run as many test cases as they'd feel comfortable with, and cycle simulators and formal verifiers aren't offering a lot of relief yet. Barbara Tuck, *Computer Design*, 1/97, p. 47, 10 pp.

Formal verification tool speeds designers to golden RTL. Modular software tool family from Chrysalis enables RTL verification to bridge the gap between functional design and implementation. Cheryl Ajluni, *Electronic Design*, 2/3/97, p. 37, 4 pp.

MEMORY

Flash memories: plenty of cheese, no mice? An overview of various flash memory architectures. Nicholas Cravotta, *Embedded Systems Programming*, 1/97, p. 71, 6 pp.

MISCELLANEOUS

The interview: Dwight Decker. Rockwell Semiconductor's president shares his views on the slow move to broadband access, the 56K-modem debates, and the outlook for wireless systems. Loring Wirbel, *OEM*, 1/97, p. 52, 4 pp.

Wearable computing: a first step toward personal imaging. Miniaturization of components has enabled systems that are wearable and nearly invisible, so that individuals can move about and interact freely, supported by their personal information domain. Steve Mann, MIT; *Computer*, 2/97, p. 25, 7 pp.

Electronic money: toward a virtual wallet. A host of technologies has been developed. Some are still theoretical, some in testing, and some in commercial use. Tekla S. Perry, *IEEE Spectrum*, 2/97, p. 18, 2 pp.

Focus report: foundries. The business cycle of the semiconductor industry changes the relationship between foundries and users. R.T. Maniwa, *Integrated System Design*, 2/97, p. 30, 4 pp.

PROCESSORS

Comparing the 251 and the XA: a kernel's perspective. Intel and Philips have introduced supercharged versions of the 8051 architecture. This article compares the two architectures based on their ability to support real-time kernels. Jean J. Labrosse, *Embedded Systems Programming*, 1/97, p. 56, 10 pp.

Microcontrollers. A sampling of recently introduced microcontrollers. *Electronic Products*, 2/97, p. 43, 5 pp.

CPU and DSP cores vie for ASIC designers' attention. Cores for 32-bit CPUs (both RISC and CISC) and DSPs are proliferating. Jim Turley, MicroDesign Resources; *Computer Design*, 1/97, p. 75, 8 pp.

Timing analysis for the PA-8000. HP engineers developed two timing-analysis methodologies to optimize the PA-8000 microprocessor. Clay McDonald, Tom Indermaur, HP; *Integrated System Design*, 2/97, p. 18, 6 pp.

PROGRAMMABLE LOGIC

Low-voltage programmables: why they've lagged, and why this is changing. The year for 3.3-V devices is upon us. Larry Waller, *Integrated System Design*, 2/97, p. 48, 3 pp.

SYSTEM DESIGN

Challenges for processor designers. The growing gap between CPU and memory bandwidth may spur the development of new DRAM designs. Maurice V. Wilkes, Olivetti; *Computer*, 2/97, p. 10, 1 pg.

Advanced microprocessors demand amperes of current at < 2 V. Future CPUs will require high current, low voltage, tight regulation, fast switching. Frank Goodenough, *Electronic Design*, 1/20/97, p. 31, 7 pp.

Designing power systems around processor specifications. Bigger and faster microprocessors demand close attention to the rules for power conversion and distribution. Steve Goodfellow, Don Weiss, Intel; *Electronic Design*, 1/20/97, p. 53, 5 pp.