by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send e-mail to belgard@umunhum.stanford.edu *with comments or questions.*

5,577,259

Instruction processor control system using separate hardware and microcode control signals to control the pipelined execution of multiple classes of machine instructions
Issued: November 19, 1996
Inventor: Merwin H. Alferness
Assignee: Unisys
Filed: August 9, 1994
Claims: 30
A pipelined processor has both hardware-controlled and microcode-controlled instructions, called complex instructions. The complex instructions are interpreted by microcode. The microcode control unit has a primary controller for executing some complex instructions and a secondary microcode controller for executing other complex instructions.

5,574,942

Hybrid execution unit for complex microprocessor
Issued: November 12, 1996
Inventors: Robert P. Colwell, et al
Assignee: Intel
Filed: February 15, 1996
Claims: 29
A hybrid execution unit in an out-of-order superscalar processor that can execute mixed data-type operations in a single cycle. Shown are certain floating-point operations that the hybrid execution unit can perform in a single cycle.

5,574,941

Computer architecture capable of concurrent issuance and execution of general-purpose multiple instruction54
Issued: November 12, 1996
Inventor: Robert W. Horst
Assignee: Tandem Computers
Filed: November 3, 1995
Claims: 4
A superscalar pipelined computer has a single pipeline that can execute each instruction of the instruction set sequentially, but only a few of the instructions in parallel.

5,574,927

RISC architecture computer configured for emulation of the instruction set of a target computer
Issued: November 12, 1996
Inventor: Henry L. Scantlin
Assignee: International Meta Systems
Filed: March 25, 1994
Claims: 25
Emulating a target architecture with a RISC architecture by decoding target instructions into a sequence of microcoded instructions and decoding the microcoded instructions into both RISC instructions and other instructions, the other instructions having indirect references to emulated target registers. The other instructions are sometimes referred to as extensions to the RISC architecture.

5,574,925

Asynchronous pipeline having condition detection among stages in the pipeline
Issued: November 12, 1996
Inventor: Nigel C. Paver
Assignee: Victoria University of Manchester
Filed: January 19, 1994
Claims: 10
An asynchronous pipeline-control mechanism uses a single bit in each stage to indicate whether a specific condition is set in that stage. A detector checks all the stages to see if the condition has been set.

5,572,689

Data-processing system and method thereof
Issued: November 5, 1996
Inventors: Michael G. Gallup, et al
Assignee: Motorola
Filed: March 21, 1995
Claims: 8
A data processor performs vector and scalar operations. The claims broadly cover a method of executing a shift instruction that conditionally shifts in a value based on two extension values and modifies one of the extension values as a result of the shift. In one claim, the shift instruction shifts in a sign bit when one extension bit is negative and shifts in the other extension bit when the first extension bit is positive.

OTHER ISSUED PATENTS

5,574,935 *Superscalar processor with a multiport reorder buffer*
5,574,928 *Mixed integer/floating-point processor core for a superscalar microprocessor with a plurality of operand buses for transferring operand segments*
5,574,871 *Method and apparatus for implementing a set-associative branch-target buffer*
5,572,700 *Cache-access controller and method for permitting caching of information in selected cache lines*
5,572,690 *Cascaded multistage counterflow pipeline processor for carrying distinct data in two opposite directions* M