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Centaur Gallops Into x86 Market

IDT Subsidiary Reveals Low-Cost 200-MHz C6 With MMX

by Linley Gwennap

Boldly entering the x86 processor market, Centaur Technology revealed at the recent PC Tech Forum its plans for a chip with the integer performance of Pentium/MMX but at a much lower cost. The new company is a subsidiary of Integrated Device Technology (IDT), which will manufacture and market the new processor. Scheduled for production shipments in 3Q97, the device will bring new levels of performance to sub-$1,200 PCs.

The chip, known as the IDT C6, is a relatively simple CPU that avoids the complex out-of-order techniques of AMD's K6 and even Pentium's superscalar design. Like a 486, the C6 issues one instruction at a time and has no branch prediction. But with large caches, an advanced TLB, and MMX compatibility, the C6 compares well with Pentium/MMX (P55C) on many PC applications. The simpler design, however, results in a 37% smaller die, reducing manufacturing cost. Simplicity also reduces power dissipation, making the C6 an excellent choice for low-cost notebooks.

As AMD and Cyrix target the high end of Intel's line, Centaur is setting its sights a bit lower, on the vast number of low-end and midrange processors that Intel ships. In these markets, price is the key buying criterion, and the C6's tiny die—smaller than any of AMD's or Cyrix's Pentium-class chips—gives Centaur a significant advantage in any price war. This advantage is likely to be called upon often, as Centaur and IDT have much less brand recognition than AMD, Cyrix, and, of course, Intel.

IDT plans to offer the C6 at speeds of 150, 180, and 200 MHz. At its top speed, the new chip matches the performance of a 200-MHz Pentium/MMX in a low-cost system configuration on the Winstone 97 benchmark, as Figure 1 shows. Like other non-Intel products, the C6 does not fare as well on floating-point and MMX-intensive applications. IDT did not announce pricing for the chip, but we expect it to debut at prices ranging from $80 to $160, at least 40% below the list price of comparable Intel processors.

Small Effort Yields Impressive Results

The ideas behind the C6 had been fermenting in Glenn Henry's mind for more than a decade. Henry became an IBM Fellow because of his pioneering efforts in RISC CPU design, including the PC/RT, but he later began searching for ways to apply RISC principles to speeding the more popular x86 instruction set. IBM wasn't interested in taking this path, however, and Henry eventually left.

After spending a few years at Dell, Henry was lured to MIPS Technologies by Tom Whiteside, another ex-IBMer, with the promise of implementing his ideas. Whiteside wanted Henry to build a half-MIPS, half-x86 processor—hence the Centaur name—that would act as the lever to pry open the PC market for MIPS (see MPR 2/14/94, p. 4). After shopping the idea to the various MIPS chip partners, however, Henry found interest at only one: IDT.

IDT set up Centaur as a separate subsidiary located in Austin (Texas). But IDT's efforts to push MIPS into the PC market were going nowhere, and both Henry and his boss, IDT CEO Len Perham, quickly realized the Centaur chip

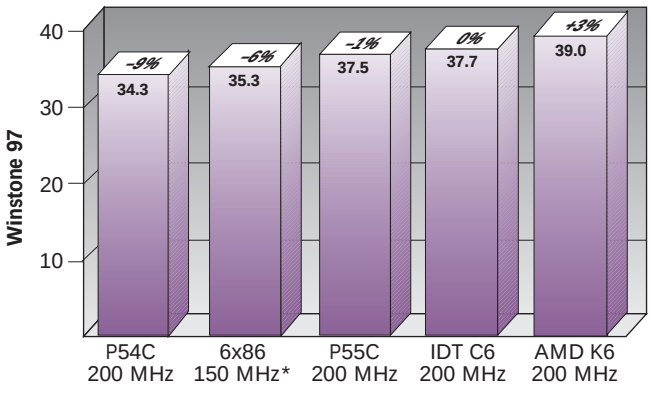

Figure 1. In a low-cost system configuration, the IDT C6 matches the performance of Intel's Pentium/MMX (P55C) at the same clock speed on the Winstone 97 Business benchmark under Windows 95. All processors tested with 256K of burst SRAM, Triton VX chip set, 32M of EDO DRAM, a WD Caviar 22100 hard drive, and a Trident 9630 2D graphics card with 1M of DRAM in 1024 x 768 x 16 mode. *PR200 (Source: Centaur)

would be more valuable without MIPS compatibility than with it. Thus, the chip became an x86-only processor.

The size and potential profitability of the x86 market interested Perham, and a second major product line could help smooth out the large revenue swings from the vendor's core SRAM business. The $500 million company couldn't afford a massive design effort for a new x86 processor, however, so Henry began work in the spring of 1995 on a shoestring budget.

He put together a relatively small team that even today numbers only about 40 engineers, recruiting experienced x86 designers from IBM and Texas Instruments along with PC experts from Dell and PowerPC engineers from Somerset. With a spectacular effort, in just under one year the team taped out an initial design, a task that often takes two to three years in other companies. In July of 1996, the chip booted Windows for the first time. Since then, Centaur has refined the design through several iterations to improve performance and compatibility.

We estimate the total cost to develop the initial C6 was $10–$15 million, perhaps one-tenth of Intel's development cost for the P6. Intel bears the cost of blazing new technology trails, while others can save money by relying on simpler, proven techniques. If the C6 attains even 1% of the total x86 market, a realistic goal for a new entrant, it will provide a solid return on this modest investment.

About half the C6 development cost was funded by NKK, which has been a second source for some of IDT's MIPS chips (see MPR 8/1/94, p. 4). The Japanese vendor has the right to market the C6 but has not yet announced plans to do so. If NKK chooses to market the C6, it will become the first x86 chip vendor based in Japan.

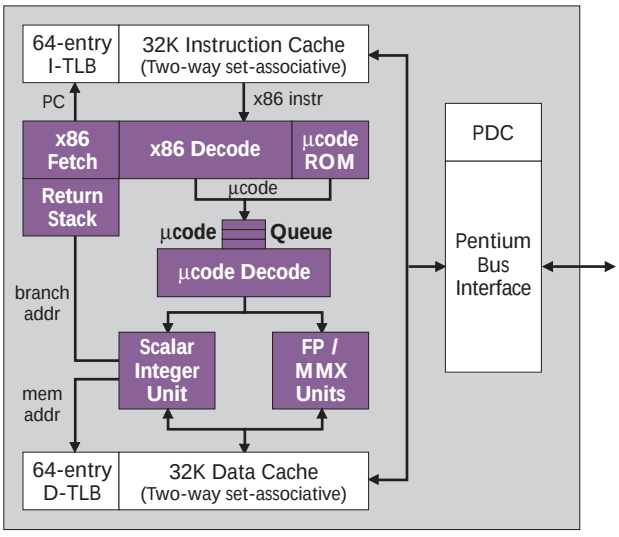

Figure 2. A block diagram of the C6 shows the simple CPU core (purple), large TLBs and caches, page-directory cache (PDC), and the Pentium-compatible bus interface.

Target: Low-Cost PCs and Notebooks

Centaur decided to target two market segments that are not being addressed well by Intel. The first is the low end of the PC market, $1,200 and below. According to Computer Intelligence, this was the fastest growing segment of the U.S. retail PC market during 1Q97. Systems at this price point are also very popular in Asia, a region that is exhibiting rapid growth in PC consumption.

Because the available profits are much lower than for its other products, Intel has shown relatively little interest in this low-cost market, declining to sell processors for much less than $100. AMD and Texas Instruments service this low-end market with the 486, but few Pentium-class options are available. In addition, smaller Asian vendors often complain about being unable to get enough processors from Intel during periods of shortage, making them more interested in non-Intel solutions.

Centaur intends to offer the performance of high-end Pentium parts, including MMX compatibility, at these low price points. This value proposition should be attractive to U.S. PC makers wanting a hot $1,000 PC, to Asian vendors tired of selling 486 systems, and to OEMs unable to get enough processors from Intel.

Unlike AMD and Cyrix, Centaur is also looking to gain notebook design wins. The C6 fits easily into the thermal envelope of most notebook PCs while offering performance similar to that of Intel's best notebook chips.

Scalar CPU Designed for High Clock Speeds

To meet the goals of low cost, low power, and short time to market, Centaur chose a simple microarchitecture. The scalar CPU decodes and executes just one instruction per cycle; as Figure 2 shows, this results in a very simple design. Almost all recent x86 CPUs have used a superscalar design to achieve better per-clock performance, but the ability of these processors to actually execute more than one instruction per cycle on real applications has been limited. The C6's scalar design has lower per-clock performance than a superscalar design but offers extensive cost savings.

In many ways, the C6 appears to be a reanimated 486

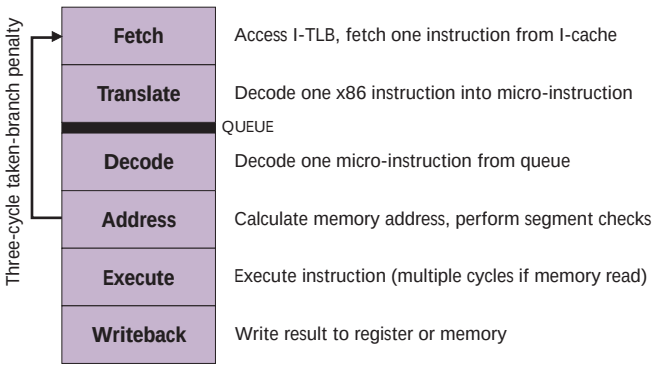

Figure 3. The C6 uses a six-stage pipeline that is similar to that of Pentium or the 486 except for the second stage.

microarchitecture. The pipeline, shown in Figure 3, is similar to the 486's except for the extra "translate" stage. This stage essentially divides the complexity of x86 instruction decoding across two pipeline stages, allowing the chip to achieve higher clock speeds. Although the initial part, at 200 MHz, is slower than the fastest Pentium/MMX, Centaur believes that once its design is fully characterized and optimized, it will exceed the clock speed of any other Pentium-class processor in a comparable IC process.

The translate stage has another benefit. Once x86 instructions are translated into internal microcode operations, these operations are stored in a three-entry queue. Since the C6, like Intel's 486 and Pentium chips, takes two or more cycles to execute instructions that operate on values in memory, this queue allows the translation unit to get ahead of the execution unit in these situations.

The translator runs asynchronously with the execution unit: that is, it does not stall when the execution unit stalls. This comes in handy because the translator itself requires an extra cycle to decode x86 prefix bytes. If there are any entries in the instruction queue when a prefix byte is encountered, the execution unit is not stalled by this delay in the translation unit. Note that the P55C has a similar six-stage pipeline and instruction queue, but the classic Pentium does not.

Pipeline Similar to P55C's

Because of the similarity in pipelines, most instructions execute in the same number of cycles on a C6 as on a Pentium. The C6, however, fares poorly on some complex instructions that are rarely used in modern code. Centaur spent little time optimizing decimal arithmetic and transcendentals (sine, etc.), for example. These and other operations execute via microcode; for this reason, the C6 microcode ROM, at 8K words, is somewhat larger than in other x86 processors.

Centaur concentrated on a few areas it believes are important for application performance. Segment loads, for example, take only two cycles, versus three on Pentium and several on AMD and Cyrix processors. Segment loads are common only in older 16-bit code, but a low-cost PC may be called upon to run these older applications.

The C6 is very quick for short string moves, with only 4 cycles of overhead, versus 13 on Pentium. Because of its single-ported cache, the C6 takes two cycles per byte, twice as many as Pentium, but for strings of eight bytes or fewer, the C6 is faster. Centaur claims that most strings are this short and that longer strings often miss the cache, eliminating the advantage of Pentium's single-cycle throughput.

On the other hand, Centaur decided not to include in its processor dynamic branch prediction, a feature found in all other x86 CPUs since 1993. Instead, the chip takes a three-cycle penalty on all taken branches. An eight-entry return stack eliminates this penalty for most subroutine returns. Centaur estimates that adding a 512-entry branch target buffer, similar to Pentium's, would have improved overall performance by about 5% but would have significantly increased the size of the die. The designers felt this tradeoff was not justified.

	IDT C6		Pentium/MMX	
	Thruput	Latency	Thruput	Latency
FP/MMX addition	1 cycle	1 cycle	1 cycle	1 cycle
FP/MMX compare	1 cycle	1 cycle	1 cycle	1 cycle
FP/MMX multiply	4 cycles	5 cycles	1 cycle	3 cycles
FP/MMX load	2–3 cycles		1 cycle	
FP/MMX store	2 cycles		2 cycles	
Max MMX per cycle	1 instr		2 instr	

Table 1. In some important areas, the floating-point and MMX timings of the C6 fall short of Pentium's performance.

Overall, the C6 integer core can be thought of as a scalar P55C without branch prediction. Since the C6 can match the performance of the 200-MHz P55C on the Winstone 97 benchmark, it appears that benchmark gains little advantage from the P55C's second integer unit and advanced branch prediction. Any benefit from these areas is counteracted by the C6's larger caches. By eliminating these complex P55C design features, Centaur gains a much smaller die size and, if its promises hold true, a higher clock speed as well.

Floating-Point, MMX Throughput Weak

Centaur admits it cut some corners in the C6's floating-point and MMX units. As Table 1 shows, the C6 does well on basic floating-point instructions such as add or compare, but the chip has a small multiplier that takes four cycles to complete, with no provision for pipelining these operations. In contrast, Pentium can complete a floating-point multiply every cycle, with a three-cycle latency. Multiplication is heavily used in many FP applications, such as 3D graphics, audio, and video processing.

The C6 has a separate MMX unit, added late in the development cycle, but shares the same registers for FP and MMX data. As a scalar processor, the C6 can execute only one MMX instruction per cycle, whereas Pentium/MMX can execute two in parallel. Because MMX instructions typically occur in inner loops, where they can be paired by hand, this ability can give the Pentium chip a performance advantage on some applications.

The MMX multiplier is as slow as the FP multiplier, hampering these applications as well. The new chip also requires at least two cycles to load FP or MMX data, whereas Pentium/MMX can load such data in a single cycle (actually, up to two loads per cycle).

There are few mainstream PC applications available today that make heavy use of FP or MMX operations, and those that do still use integer instructions for the bulk of their code, so the C6's overall performance will be better than the numbers in Table 1 imply. Other non-Intel chips also lag Intel's processors on FP and MMX programs.

Interest in 3D games (powered by floating-point operations) and MMX-based multimedia is growing, but Centaur points out that low-end PCs will be the last to move to these

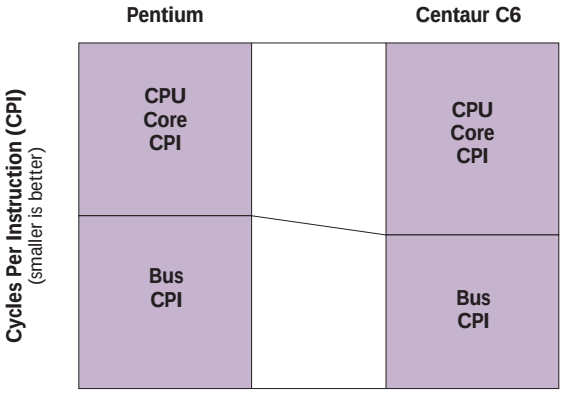

Figure 4. Compared with a Pentium, the C6 has a slower CPU but spends less time waiting for the bus, resulting in roughly equivalent performance on many applications.

leading-edge applications. Since these PCs typically have no 3D-graphics acceleration, adding a modest 3D card to a C6-based system will result in better 3D performance than a Pentium/MMX system with no 3D card, yet the C6 system will still cost less. With Intel relentlessly promoting the FP and MMX performance of its processors, however, some buyers will be wary of this argument (see MPR 6/2/97, p. 32).

Breaking the Bus Bottleneck

Given the limitations of its scalar CPU core, what really differentiates the C6 is its cache and bus architecture. The C6 has on-chip instruction and data caches of 32K each, twice as much as Pentium/MMX and four times as much as a standard Pentium (P54C). These caches are two-way set-associative and, as in most x86 processors, efficiently handle the unaligned accesses common in x86 code.

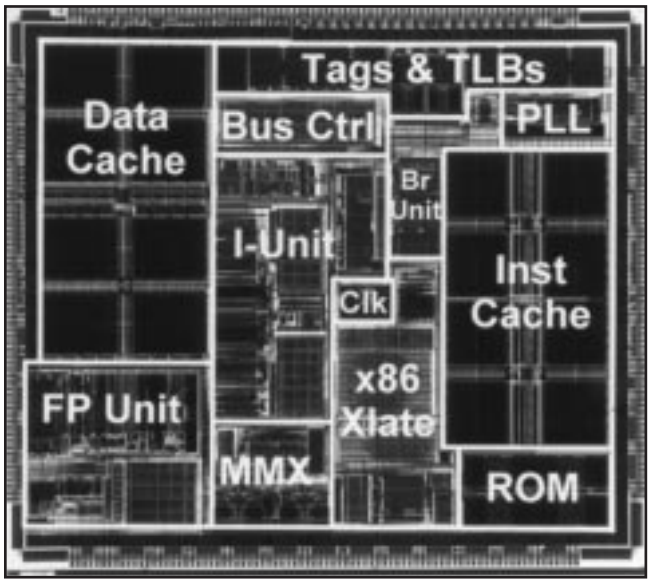

Figure 5. The production version of the Centaur C6, shown in this die plot, contains 5.4 million transistors (4.0 million in the caches) and measures 10.2 mm × 8.6 mm when manufactured in IDT's 0.28-micron CMOS-9+ process. (The version currently sampling is slightly larger due to extra debug circuitry.)

These caches are simpler than in other competitive chips. For example, virtually all other Pentium-class processors have a dual-ported data cache; to match its scalar core, the C6 has a single-ported data cache, reducing die area. The C6 also has no predecode bits in the instruction cache, a feature found in Pentium (but not Pentium/MMX) and AMD's K5 and K6. These extra bits cause the caches on these chips to consume more die area than the same amount of cache on the Centaur chip.

Like all other Intel competitors, Centaur designed its chip to fit into the P55C's Socket 7, allowing it to work with a variety of system-logic chip sets and motherboards from Intel and third parties. Centaur realized, however, that the limited bus bandwidth of Socket 7 is the biggest performance bottleneck in most PCs today. A Pentium-200, for example, spends about half of its time waiting for the bus, due to either an L2-cache, main-memory, or I/O transaction.

Rather than trying to match the performance of Pentium exactly, Centaur has used its transistor budget for bigger caches and TLBs instead of a complex CPU core. This tradeoff reduces the amount of time the chip spends waiting for the bus while extending the time required for the CPU to complete some calculations. The net effect, as Figure 4 shows, is roughly equivalent performance, at least on Winstone 97. The different tradeoffs will cause performance to vary, however, depending on how CPU-centric the application is.

The first step in reducing the effect of the bus is the larger caches. The larger caches have a better hit rate than the caches on Intel's chips, resulting in fewer bus accesses. (For the same reason, both AMD and Cyrix have also packed 64K of cache onto the K6 and 6x86MX, respectively.)

Another major source of bus accesses is TLB misses. The C6 has separate four-way set-associative instruction and data TLBs, each with 64 entries. The instruction TLB is twice as large as Pentium/MMX's, although the data TLB is the same size. As with the caches, the larger size reduces the number of misses.

More important and unusual is a page-directory cache (PDC). The x86 architecture defines a two-level address translation that requires the processor to first fetch the page-directory entry, then the actual physical address. The PDC holds eight entries from the page directory. Since each entry covers 4M of physical address space, the PDC has a typical hit rate of more than 90%. By eliminating one of the two memory accesses required to process a TLB miss, the PDC cuts the miss penalty almost in half.

The 6x86 has a similar page-directory cache. Cyrix, however, says this feature is typically turned off, as it can cause compatibility problems with some software. If Centaur runs into the same problem, its performance may suffer.

Simple Design Reduces Cost

With its simple design, the C6 has a low manufacturing cost.

The die, shown in Figure 5, measures just 88 mm^2, slightly smaller than a P54C Pentium and much smaller than any other Pentium- or P6-class x86 chip. IDT will manufacture the C6 in its CMOS-9+ technology (see MPR 9/16/96, p. 11), which combines 0.28-micron transistors with the metal layers of a 0.35-micron process.

Although the drawn gate length of this process is similar to that of AMD's CS-34EX (used for the K6) and Intel's P854 CMOS process (used for Pentium/MMX), the IDT process has a lower wafer cost, further increasing the C6's cost advantage. AMD's process is more expensive, due to its fifth metal layer and local interconnect. The Intel process has tighter metal pitches and uses trench isolation, both of which also increase wafer cost. If the C6 were built in Intel's process, it would be faster and significantly smaller.

The MDR Cost Model estimates the C6 will cost $40 to manufacture, about the same as a P54C Pentium but less than other competitive chips, as Table 2 shows. This cost savings is achieved through the simpler design of the C6. For example, Pentium has two complete integer pipelines, duplicating decode logic and execution units. Additional logic is required to determine if pairs of instructions can be executed together and to arbitrate between the two execution units. Pentium also sports a dual-ported cache to allow two x86 instructions to access memory simultaneously. The C6 avoids all of this complexity and instead devotes additional die area to the on-chip cache.

Intel's P6 CPU, with its instruction-reordering logic, is even more complex than Pentium. AMD's K6 is similar to the P6 in its ability to translate x86 instructions into RISC-like operations and execute these operations out of order. The K6 also features instruction predecoding, which bloats the size of the instruction cache. Cyrix's 6x86MX lies somewhere between Pentium and the P6 on this complexity axis. All of these chips deliver slightly better performance than the C6 on many PC applications, but by eliminating all of these advanced features, the Centaur chip has a far lower cost.

Suitable for Notebooks and Desktops

Like Intel, IDT plans to sell both desktop and mobile versions of its processors. The desktop version comes in a 296-pin PGA compatible with other Socket-7 processors. The 200-MHz version uses a 3.52-V supply, the maximum allowed in Socket 7, and dissipates 14 W (maximum). The company plans to deploy 150- and 180-MHz versions of the part that operate at 3.3 V and use somewhat less power.

Although the mobile C6 uses the same die as the desktop version and operates at the same supply voltages, it is programmed via laser to enable additional dynamic power-management features, allowing IDT to charge a premium for these parts. These features reduce the maximum power of the 200-MHz version to 10.6 W, still a bit high for most notebooks. More important, the mobile C6 dissipates just 8.4 W at 180 MHz and 7.1 W at 150 MHz, well within the thermal envelope of most notebook PCs. In fact, with a 15% lower power consumption than a Mobile Pentium/MMX of the same speed grade, the C6 will provide a slight increase in battery life for notebook vendors that adopt it.

Price & Availability

IDT has not announced pricing for the IDT-C6. The company is now sampling the part at speeds of 150, 166, and 200 MHz and expects general shipments to begin in 3Q97. For more information, contact Integrated Device Technology (San Jose, Calif.) at 408.727.6116, try its fax-back service at 1.800.943.8329, or access the Web at *www.centtech.com/prodinfo/welcome.html.*

The mobile C6 uses the same PGA package as the desktop part. Although most larger notebook makers have moved to Intel's TAB package or the new Mobile Module, the smaller vendors IDT is targeting continue to build PGA-based notebooks. Unlike the K6, whose C4 bonding makes it incompatible with TAB, the C6 could easily fit into a TAB package or module in the future, if required by its customers.

Neither AMD's K-series processors nor Cyrix's 6x86 chips have low enough power for a typical notebook system. These vendors are currently concentrating on the larger desktop market. Both vendors may offer notebook chips in 1998, after they move to 0.25-micron processes with lower supply voltages.

In the notebook space, the strongest competitor for the C6 will be Intel's Tillamook (see MPR 5/12/97, p. 4),

	Centaur C6	Intel Tillamook	AMD K6	Cyrix M2
Clock speed	200 MHz	233 MHz*	233 MHz	188 MHz
Pipeline	6 stages	6 stages	6 stages	7 stages
Decode rate	1 x86	2 x86	2–3 x86	2 x86
Issue rate	1 x86	2 x86	6 ROPs	2 x86
MMX issue	1 instr	2 instr	1 instr	1 instr
Reorder buffer	None	None	24 ROPs	None
Reg renaming	None	None	32 regs	32 regs
Branch history	None	256 entries	8K entries	512 entries
Return stack	8 entries	4 entries	16 entries	8 entries
Cache (I/D)	32K / 32K	16K / 16K	32K / 32K	64K unified
TLB (I/D)	64 / 64	32 / 64	128 unified	16 + 384 L2
Page dir cache	Yes	No	No	Yes
Core voltage	3.3/3.52 V	1.8 V*	2.9/3.2 V	2.8 V
Max power	14 W	7 W*	29 W	18 W
Transistors	5.4 million	4.5 million	8.8 million	6.5 million
Die size	88 mm^2	90 mm^2*	162 mm^2	197 mm^2
IC process	0.28µ, 4M	0.25µ, 4M	0.3µ, 5.5M	0.33µ, 5M
Mfg cost*	$40	$45	$70	$80
Availability	3Q97	3Q97	2Q97	2Q97
List price	$80–$200*	$400–$600*	$244–$469	$190–$320

Table 2. The C6 stacks up well against Intel's forthcoming 0.25-micron P55C, code-named Tillamook, and has a much lower cost than either AMD's K6 or Cyrix's 6x86MX (M2). The IDT processor is likely to sell for a much lower price than any of these competitive products. (Source: vendors except *MDR estimate)

due in 3Q97. Tillamook is expected to reach speeds of 233 MHz and dissipate about 7 W. Centaur plans to reduce the supply voltage of its mobile parts to 2.8 V later this year, allowing it to match the lower power dissipation of Tillamook, and expects to increase the clock speed of the C6 as well. Even if the mobile C6 can't match Tillamook in sheer performance, it should easily provide a price/performance advantage.

Rapid Improvements in Future

Although the C6 is impressive in its own right, the part represents only the initial effort of a design team rushing to get a product to market. Speaking at the recent PC Tech Forum, Glenn Henry said his team is already hard at work refining the initial design and will deploy an improved version within 6–9 months of the first product. Some of the changes are aimed at improving overall performance by 20–30%, but the biggest changes will be in the floating-point and MMX units. By reworking the slow multiplier and addressing other weaknesses of the initial FPU, the team may be able to boost performance on FP and MMX operations by as much as 2×.

THE PHOTO GROUP

Centaur founder Glenn Henry unveils his new company and its x86 processor at the PC Tech Forum.

By 1H98, IDT will have a 0.25-micron CMOS-10 process available, improving clock speed and greatly reducing the size of the die. Combined with the improved core, this process could produce a part at more than 300 MHz with low-end P6 performance. The challenge, however, will be to maintain high application performance within the confines of Socket 7.

As the CPU speed goes up, the demands on the external bus rise as well. To counter this effect, Centaur plans to move to 75-MHz and faster buses, taking advantage of the work of AMD and Cyrix, as well as third-party chip-set makers, to develop these higher bus speeds. Ultimately, Centaur plans to use IDT's memory technology to integrate the entire L2 cache onto the processor, greatly reducing bus traffic. Even in the current CMOS-9 technology, a C6 with an integrated 256K L2 cache would require only about 160 mm^2, according to Henry. In CMOS-10, such a chip would measure less than 100 mm^2.

Since we expect Intel to be shipping 400-MHz Pentium II processors in 1998, Centaur will remain behind Intel's leading edge. These projected improvements, however, should allow Centaur to continue to offer the performance of Intel's midrange products within the cost of a $1,200 PC, assuming the fledgling vendor can deliver.

Strong Competitive Position

IDT has not announced pricing for the C6, so a precise comparison with current products is difficult. We expect the C6 to be priced at least 40% below the price of competitive Intel products, given that AMD and Cyrix offer similar discounts. Given our projections of 3Q97 Intel pricing, that would put the C6-150 at less than $80, the C6-180 below $120, and the C6-200 below $160. Since Intel charges a premium for its mobile chips, IDT could probably do the same.

Given our manufacturing cost projections, these prices still leave a nice profit margin for IDT. The company will have to match Intel's price cuts over time, but since Intel's minimum list price is $106, the lowest price IDT would have to offer to maintain a 40% discount would be $65, which still allows a reasonable profit, particularly compared with the margins on IDT's SRAMs.

When IDT moves the C6 to its 0.25-micron process, its costs will be even lower. In fact, at that point, the C6 could move into non-PC applications such as network computers and other embedded devices. The 486 is popular in some high-end embedded applications today, and even Pentium is creeping into the embedded space, so there will be demand for a Pentium-class CPU at the price points enabled by the C6's small size. With TI's departure from the x86 market and other x86 vendors focused on the more profitable desktop, the C6 could find a nice niche in the embedded world.

Its impressive cost/performance ratio should provide the C6 with moderate success in the PC market, probably enough to meet the company's modest goals. There are several barriers, however, to the chip's sales. Perhaps the biggest is that, while many PC makers buy SRAMs from IDT, the chip vendor has no track record as an x86 processor supplier. Cyrix took years to build its brand awareness and credibility; IDT is well behind in this area.

Centaur may also run into legal barriers. Intel has sued every other company that has brought an x86-compatible processor to market. Given Intel's current legal troubles (see MPR 6/2/97 p. 26), it may make an exception for Centaur, but there's no guarantee. IDT is building the chips itself and has no Intel patent license (neither does NKK), so it lacks the protections used by AMD and Cyrix. Centaur claims its design does not infringe on any Intel patents, but Intel is likely to have a different opinion. IDT could also follow Cyrix's footsteps and assert its own patents against Intel. Even if IDT were to eventually win such a case, however, an extended legal action could severely tax its resources.

If Centaur can clear these barriers, it should attract enough business to justify IDT's ongoing investment. Given the company's limited fab capacity, even in the best case it seems unlikely to approach AMD's or Cyrix's market share in the next few years. But with a strong product, IDT is well positioned to find a niche in the huge and hugely profitable x86 market. M