Cyrix 6x86MX Outperforms AMD K6

Former "M2" Delivers Strong Performance, Adds MMX to Cyrix Repertoire

by Linley Gwennap

Intel's competitors continue to turn up the heat on the x86 giant. Following AMD's recent K6 announcement, Cyrix and IBM Microelectronics today announced volume availability of their 6x86MX processor, code-named M2. This chip extends the performance of the original 6x86 by increasing its clock speed and adding a larger on-chip cache. The new chip is also Cyrix's first to incorporate Intel's MMX multimedia extensions.

The 6x86MX relies on the same superscalar CPU core as the original 6x86 (M1), which does not implement the advanced instruction translation and reordering found in Intel's P6 processors or AMD's K6. Surprisingly, the relatively simple CPU delivers better performance on typical PC applications than either of these cores on a clock-for-clock basis. Based on the Winstone 97 benchmark, the 6x86MX, at its maximum speed of just 188 MHz, outperforms a 233-MHz K6 or a 233-MHz Pentium/MMX and approaches the performance of a 233-MHz Pentium II.

Cyrix is quickly converting all of its production to the new part, obsoleting the non-MMX 6x86. The new chip revitalizes Cyrix's lineup in the face of Intel's MMX onslaught, allowing Cyrix to compete with Pentium/MMX up and down the line while edging into Pentium II's range. By moving the 6x86MX into IBM's more advanced process technologies over the next year, the two vendors plan to offer parts that further overlap Intel's Pentium II line.

6x86MX Does Well on Winstone 97

Although the company has dropped its supercilious "+" suffix, Cyrix continues to use the PR (performance rating) nomenclature for its chips, whose clock speed is not an adequate representation of their relative performance. For the new chips, the company slightly redefined the PR rating, which originally referred to Pentium (P54C) performance. Today's market is more complicated, as Pentium/MMX (P55C) offers better per-clock performance than the P54C, and the K6 offers more performance than the P55C at the same clock rate. Cyrix's new PR rating encompasses all of these competitors.

Both Cyrix and IBM announced three speed grades for the 6x86MX: PR166, PR200, and PR233. These parts operate at core CPU speeds of 150, 166, and 188 MHz, respectively. All the parts use a 2.5× bus-clock multiplier for best performance, with the 188-MHz CPU relying on a 75-MHz bus, although slower speeds are supported if desired.

Figure 1 shows Cyrix's performance positioning, based on mainstream PC applications under Windows 95. The data shows the 6x86MX-PR166 outperforming a K6-166 by 3% and a P55C-166 by 8%. Cyrix's PR200 and PR233 outscore the corresponding K6 and P55C chips by a similar margin. According to Cyrix, its PR233 chip comes within 1% of a 233-MHz Pentium II on this benchmark.

Figure 2 shows similar data under Windows NT. In this case, the Cyrix chip comes in about 3% ahead of Pentium/MMX and the K6. Pentium II gets a small boost on Windows NT, putting the 233-MHz part about 3% above the fastest 6x86MX.

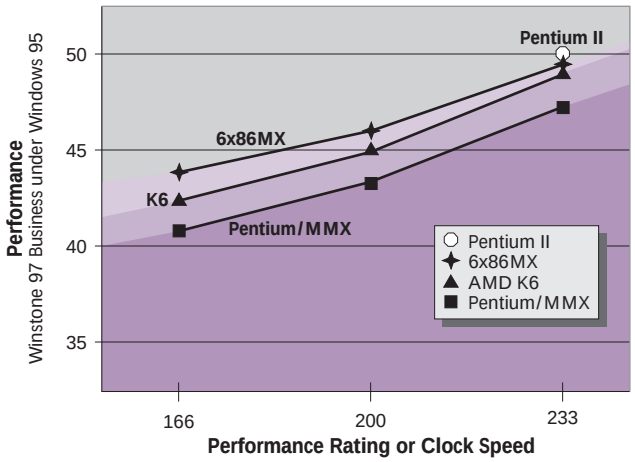

Figure 1. On the Winstone 97 Business benchmark running under Windows 95, the 6x86MX outperforms Pentium/MMX and AMD's K6. All processors tested with 512K of cache, SiS 5571 chip set (except 440FX for Pentium II), 32M EDO DRAM, Quantum Fireball ST32A011 hard drive, and STB Nitro 3D graphics accelerator with 4M of VRAM in 1,024 x 768 x 16 mode. (Source: Cyrix)

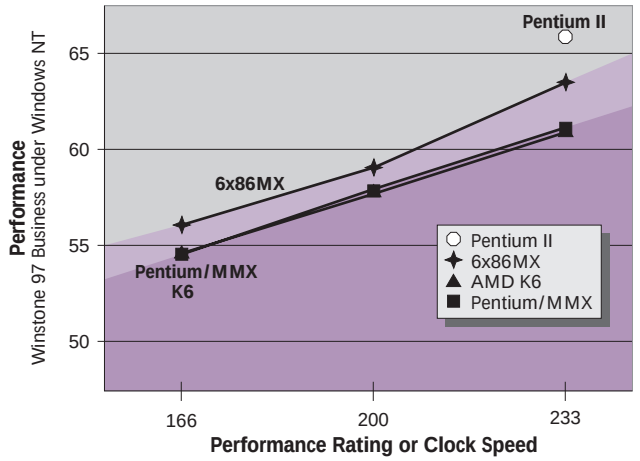

Figure 2. When tested under Windows NT, the 6x86MX has a smaller advantage over Pentium/MMX but still outperforms both it and the K6 on the Winstone 97 Business benchmark. A 233-MHz Pentium II outscores the Cyrix PR233 by about 3%. System configurations are the same as in Figure 1 except K6 uses Triton 430TX. (Source: Cyrix except K6 from *PC Magazine Online*)

Given this data, Cyrix's PR ratings are actually a bit conservative when compared against Pentium/MMX, particularly under Windows 95, where Cyrix's PR166 actually outruns a P55C-200. The ratings position Cyrix well against both Pentium/MMX and AMD's K6, a key competitor, under either of the two popular PC operating systems. As Cyrix introduces faster versions of the 6x86MX, it presumably will adjust the PR number to match up against Pentium II.

Performance on many MMX- and floating-point-intensive applications will lag the PR rating. A lack of accepted benchmarks in these areas hinders the comparison, but Cyrix released data showing the 6x86MX to be about the same as or slightly slower than Pentium/MMX on image manipulation (MMX) and 3D games that use floating-point math. Pentium II is significantly better than Pentium/MMX on most FP applications, so the 6x86MX is likely to fall well behind Intel's top of the line in this area.

Simpler Design Outperforms Complex Ones

Cyrix's figures show that a 166-MHz 6x86MX (PR200) outperforms a P55C-166 by 8–13% on Winstone 97, depending on the operating system. The Cyrix chip has two clear advantages over the P55C design. First, the 6x86 core features register renaming and an extra pipeline stage (see MPR 10/25/93, p. 1) that reduces stalls compared with the P55C. Second, the P55C spends a large percentage of its time waiting on the system bus; the 6x86MX reduces this wait time with its larger on-chip cache and TLB.

As Table 1 shows, the new Cyrix chip features 64K of on-chip cache, twice as much as the P55C. The unified design of the 6x86MX cache further improves its hit rate compared with the split instruction and data caches on the P55C. The 6x86MX also includes a generous 400-entry TLB. Although 384 of these entries are in the second-level TLB and take an extra cycle to access, this structure reduces memory accesses, particularly for Windows NT, compared with the P55C.

The real surprise is that, on typical PC applications, the 6x86MX outperforms more complex designs such as AMD's K6 and Intel's Pentium II (PII) on a clock-for-clock basis. With both chips operating at 166 MHz and using a 66-MHz bus, the 6x86MX delivers 8% more performance than the K6 on Winstone 97, according to Cyrix. Comparing it with Pentium II is more difficult, since the two chips have no frequencies in common, but given that Cyrix's 188-MHz part is similar to the PII-233 in performance, a 233-MHz 6x86MX would surely outperform the PII-233 on this test.

The K6 has the same amount of on-chip cache as the 6x86MX, although again Cyrix's unified design gives it a slight edge in cache hit rate. Cyrix's larger TLB provides another small edge, but the 6x86MX core still appears to be outperforming the K6 core, which includes more extensive parallel and out-of-order execution.

The 233-MHz Pentium II has a highly touted dual-bus architecture featuring a 117-MHz fully pipelined L2 cache plus a 66-MHz system bus. Although the 6x86MX is stuck in the Pentium-compatible Socket 7, it can access its L2 cache at up to 75 MHz, just a third slower than Pentium II, and can often pipeline its cache accesses as well. With twice the on-chip cache of Pentium II, the 6x86MX apparently makes up for the slower L2 cache and lack of a separate main-memory bus, at least on the Winstone 97 suite. Even if one assumes the 6x86MX's cache architecture has a slight edge over Pentium II's, that still means the 6x86 core is matching the per-clock performance of Pentium II's P6 core, which has even greater instruction reordering capabilities than the K6.

	Cyrix 6x86MX	Intel P55C	AMD K6	Intel Pentium II
Clock speed	188 MHz	233 MHz	233 MHz	266 MHz
Pipeline	7 stages	6 stages	6 stages	12–14
Decode rate	2 x86	2 x86	2–3 x86	3 x86
Issue rate	2 x86	2 x86	6 ROPs	5 ROPs
MMX issue	1 instr	2 instr	1 instr	2 instr
Reorder buffer	None	None	24 ROPs	40 ROPs
Reg renaming	32 regs	None	32 regs	48 regs
Branch history	512 entries	256 entries	8K entries	>512?
Return stack	8 entries	4 entries	16 entries	4 entries
Cache (I/D)	64K unified	16K / 16K	32K / 32K	16K / 16K
TLB (I/D)	16 + 384 L2	32 / 64	128 unified	32 / 64
Core voltage	2.8 V	2.8 V	2.9/3.2 V	2.8 V
Max power	18 W	17 W	29 W	27 W*
Transistors	6.5 million	4.5 million	8.8 million	7.5 million
Die size	197 mm²	128 mm²	162 mm²	203 mm²
IC process	0.33µ 5M	0.28µ 4M	0.3µ 5.5M	0.28µ 4M
Mfg cost*	$80	$50	$70	$90
Availability	Now	Now	Now	Now
List price	$190–$320	$270–$598	$244–$469	$636–$775†

Table 1. The 6x86MX is less expensive than its rivals but delivers similar performance despite its lower clock speed. †includes 512K L2 cache (Source: vendors except *MDR estimate)

Reordering Requires More Parallelism

The 6x86 core's key advantage is its extra pipeline stage, which fetches operands from the data cache the cycle before they are needed for instruction execution. This change permits x86 instructions that operate on memory to flow smoothly through the pipeline without delays. For example, the instruction ADD [mem], CX loads a value from memory, adds it to the contents of CX, and stores the result to memory. This instruction executes in a single cycle in the 6x86 but takes three cycles to execute in the P55C.

The K6 and P6 use a very different design. Both CPUs convert complex x86 instructions such as this one into a series of RISC-like operations (ROPs). The above instruction would be converted into three ROPs: a load, an add, and a store. Obviously, these three ROPs must be executed sequentially, since there are strict dependencies. The complete execution time is thus three cycles, just as in the P55C.

To offer a performance gain, the K6 and P6 must execute other instructions in parallel with this series of ROPs. The reordering capabilities of these chips are intended to

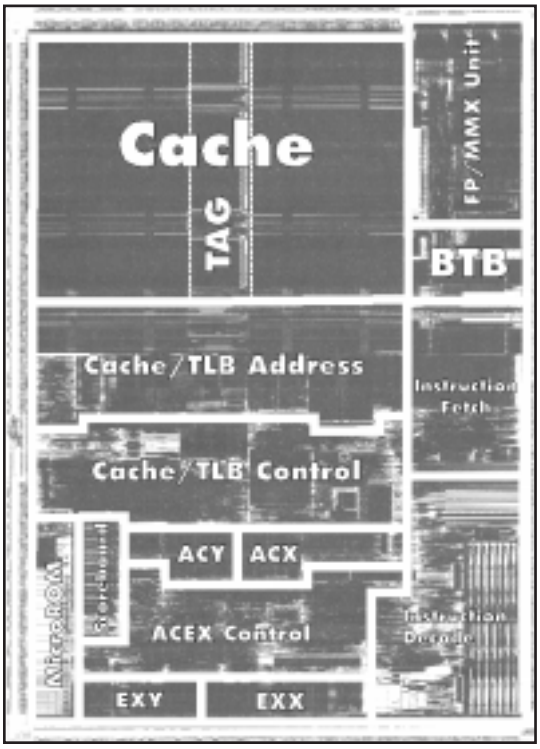

Figure 3. With 6.5 million transistors, the 6x86MX measures 11.9 × 16.3 mm in IBM's 0.33-micron five-layer-metal process. The layout is represented here by a die plot, since the fifth metal layer in the die photo obscures most details.

increase parallelism by locating nondependent ROPs further down the instruction stream and promoting them. The P6, for example, examines up to 20 ROPs at once to find ones that can be issued in parallel.

Apparently, the programs and workloads represented by Winstone 97 do not provide enough inherent parallelism to allow the P6 and K6 to reach their performance potential. If the instruction streams contain many dependencies and the instructions themselves are broken down into dependent ROPs, the opportunities for parallel execution are limited. In this environment, the 6x86 design shines.

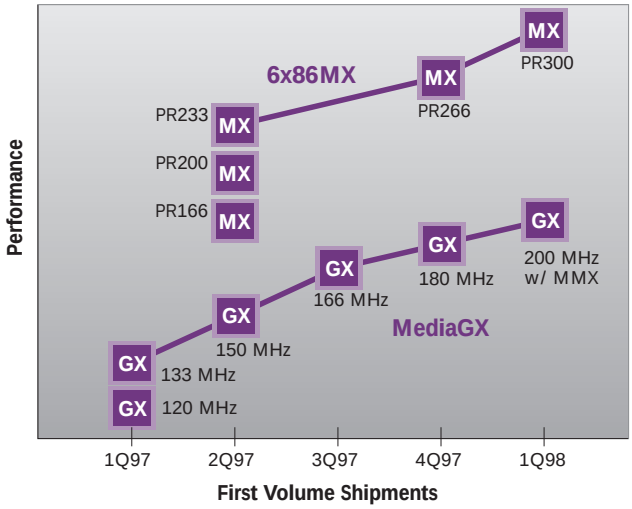

Figure 4. Cyrix's roadmap includes two process shrinks, the first resulting in a PR266 version and the second in a PR300 part. Improving process technology will also boost the MediaGX's clock speed over time, filling in the low end. (Source: Cyrix)

The 6x86 has the further advantage of being able to process two memory reads per cycle, using its dual-ported cache. The P6 and K6 can handle only one load per cycle, although each can pair the load with a store. Because of its tiny register set, x86 code is naturally load-intensive, generating an average of 0.6 loads per instruction on typical applications. This pressure can create a load bottleneck in processors like the P6 when it attempts to execute two or more instructions per cycle.

The tradeoff of the 6x86 design is in clock speed. The RISC-like core of the P6 operates at up to 266 MHz, 40% faster than the top speed of the 6x86MX. Although some of this edge is due to Intel's superior manufacturing technology, we estimate the P6 has an inherent 10–20% clock-speed advantage due to its RISC-like design and longer pipeline. The K6 has been announced at 233 MHz, 24% faster than the 6x86MX in a more similar manufacturing process, although AMD has yet to begin volume shipments at that clock speed. Time will tell whether its clock-speed edge will hold.

Cyrix had initially hoped its 6x86MX would reach speeds of 225 MHz (see MPR 10/28/96, p. 23), better positioning the chip to compete against high-end P6 processors. The company now hopes its per-clock performance advantage will balance out its lower clock speeds.

Process Shrinks Will Boost Performance

The initial 6x86MX, shown in Figure 3, measures 197 mm^2 in IBM's 0.33-micron CMOS-5X process. As Table 1 shows, this die size is larger than that of any other P55C-class processor and about the same as Pentium II. The metal pitches of CMOS-5X (see MPR 7/10/95, p. 16) are much larger than in Intel's or AMD's 0.35-micron processes, however, so this comparison is not quite fair. The 6x86MX would be smaller than the K6, for example, if built in a similar process. Still, the older process is not cost-effective: according to the MDR Cost Model, the 6x86MX costs about $80 to build, 15% more than the K6.

The 6x86MX uses a 2.8-V core, like the current 6x86L parts, easing the impact on motherboard makers. At that voltage, the PR233 version dissipates a maximum of 18 W, making it cooler than either the K6 or Pentium II, both at nearly 30 W, and about the same as Pentium/MMX. Previous 6x86 chips had dissipated as much as 25 W, causing some PC designers to sweat. The new chip, thanks to a process shrink and the larger on-chip cache, solves that problem, but even a slower, voltage-reduced version would still be a bit too hot for notebook designs. Cyrix has no plans to offer a version of its chip for notebook systems, at least though 1997.

Cyrix is working with IBM to apply more advanced process technology to the 6x86MX, resulting in two process

shrinks, as Figure 4 shows. Around the end of this year, Cyrix plans to ship a PR266 version of the 6x86MX built in IBM's 0.25-micron CMOS-6S2 process (see MPR 9/16/96, p. 11). We expect this move will reduce the die size of the chip to about 120 mm^2 and boost the clock speed to at least 225 MHz, supporting a PR266 rating (comparable to PII-266). This version will retain the 2.8-V core supply.

A second process shrink, to CMOS-6X, will provide additional benefits in 1H98. The transistors in CMOS-6X are similar to those in CMOS-6S2, but the metal pitches are further reduced. In CMOS-6X, the 6x86MX could shrink to less than 80 mm^2. The new process would offer a slight boost in clock speed, allowing a PR300 part. Cyrix has not specified the clock speed of this part, but a 250-MHz CPU with an 83-MHz bus might fit the bill. CMOS-6X carries a nominal core voltage of 1.8 V, which will force system designers to make a change but allow the 6x86MX to potentially move into notebooks as well as desktops. We expect Intel to move Pentium II to a 1.8-V core in 1H98, paving the way for others to adopt the same voltage.

This roadmap should nearly halve the chip's manufacturing cost over the next year, but the proposed performance boost is only from PR233 to PR300. In the meantime, we expect Intel to move Pentium II to 400 MHz and AMD to push its K6 above 300 MHz by early 1998, raising the bar for Cyrix. Even newcomer IDT (see MPR 6/2/97, p. 1) may be nipping at Cyrix's heels with a 300-MHz part by mid-1998.

Cyrix has not discussed its plans beyond this point. Other Socket 7 vendors are considering integrating an L2 cache onto the CPU next year, and CMOS-6X would allow Cyrix to follow suit. The company is also working on a next-generation processor code-named M3; this device should provide a large performance boost sometime in 1999.

Aggressive List Pricing Undercuts AMD

Cyrix is offering discounts of up to 50% off Intel's list price for comparable parts despite the 6x86MX's integer performance edge. The PR200, at $240, is less than half the price of the $492 P55C-200. Being the middle speed grade, the PR200 is likely to make up the majority of Cyrix's product mix. The PR233, at $320, is priced about 45% below Intel's new 233-MHz P55C (see MPR 6/2/97, p. 4). Of course, Intel will rapidly bring down the price of its Pentium/MMX parts over the next few quarters, and Cyrix will have to respond to maintain its edge. IBM is also selling the 6x86MX, but its list prices are considerably higher than Cyrix's (see sidebar).

Cyrix's initial pricing for the 6x86MX is about 20% below AMD's K6 pricing. Since those accounts willing to consider a non-Intel processor are likely to examine the K6 and 6x86MX side by side, AMD will be forced to justify its higher prices. With AMD trying to gain market share and fill its enormous Fab 25, the company is likely to offer significant discounts in order to win designs against Cyrix.

Both IBM and Cyrix are aiming the new part at PCs that sell for $1,200 to $2,000. As Intel cuts its prices, the performance points for these PCs will increase over time. Thus, Cyrix must keep pace with its performance roadmap to maintain price stability in its overall product line. If Cyrix falls behind its plans, Intel's price cuts will force it to drop the price of its own processors, reducing its average selling price. The 6x86's deficiencies in floating-point and MMX performance may also cause its prices to sag over time if Intel succeeds in convincing PC buyers that these factors are important (see MPR 6/2/97, p. 32).

Implementing the roadmap is also necessary for Cyrix to continue increasing its revenue. The company has been receiving a fixed number of wafers per month from IBM and no wafers from SGS-Thomson; assuming these trends continue, Cyrix's only way to increase unit output is to reduce the die size of its part. In the short term, Cyrix may actually see a drop in unit shipments as it converts from the old 6x86 to the larger 6x86MX, but the increase in selling price should more than make up for it.

Cyrix and IBM hope to build on the success of the 6x86. Although that part had problems when initially launched at Intel-like prices, sales perked up last fall when the companies began offering massive discounts (see MPR 12/30/96, p. 1). To date, the two vendors have sold more than five million 6x86 chips to second- and third-tier PC makers. The biggest customers are AST (now part of Samsung), Acer, CTX, Cybermax, Fujitsu, IBM (only in its European PCs), and Vobis, the largest PC maker in Germany.

With the surprisingly good performance of the new 6x86MX, Cyrix has re-established itself as a strong competitor to AMD. Both companies will work together to extend the life of Socket 7 even as they compete with each other to fill that socket in midrange PCs. Although AMD was the first to market with an MMX-enabled part, Cyrix has come out swinging with lower prices. This could signal the start of a bruising price war among Intel's competitors. M

Price and Availability

Both Cyrix and IBM offer the 6x86MX in speed grades of 150, 166, and 188 MHz, called the PR166, PR200, and PR233, respectively. Cyrix is offering the PR166 and PR200 with immediate volume availability; the PR233 is in limited production, with full volume expected in 3Q97. In 1,000-piece quantities, Cyrix's list prices are $190, $240, and $320, respectively. For more information, contact Cyrix (Richardson, Texas) at 800.462.9749 or 972.968.8388, or access the Web at *www.cyrix.com.*

IBM is currently sampling the 6x86MX in all speed grades, with volume production planned for 3Q97. IBM's 1,000-piece list prices are $202, $369, and $477 for the PR166, PR200, and PR233 versions, respectively. For more information, contact IBM Microelectronics on the Web at *www.chips.ibm.com/products/x86.*