## AUDIO/VIDEO

*Single-chip DVD decoders permit user customization.* A pair of DVD decoder ICs uses microcoded architecture to give users a faster way to design, differentiate, and upgrade digital-video consumer products. Paul McGoldrick, *Electronic Design*, 4/14/97, p. 148, 2 pp.

## BUSES

*Next-generation buses to drive computer telephony.* Integrators using the MVIP (Multi-Vendor Integration Protocol) bus, a voice/data-stream bus for CT, have several hundred boards to choose from. Chris Smith, Natural Microsystems; *RTC*, 4/97, p. 32, 2 pp.

*IndustryPack: challenges of the next generation—32 MHz.* Now that IndustryPack has become an industry standard for mezzanine cards, its 8-MHz speed needs improvement. Kim Rubin, Greenspring Computers; *RTC*, 4/97, p. 112, 3 pp.

*To USB, or not to USB?* That is the question—whether 'tis better to embed it in your design or suffer the slings and arrows of outrageous market demands. Tom Cantrell, *Computer Design*, 5/97, p. 82, 5 pp.

*SCSI evolves to meet changing, challenging demands of small computers.* The SCSI standards committee refuses to stand by and watch advances in the small-computer market pass it by. SCSI advances have met the high-speed challenge head-on. Erich Otto, Symbios; *EDN*, 5/8/97, p. 155, 4 pp.

## DSPS

*EDN's 1997 DSP-architecture directory.* This directory describes 30 general-purpose DSP architectures and guides you through the maze of choices as you determine the best DSP for your next design. Markus Levy, *EDN*, 5/8/97, p. 42, 32 pp.

## IC DESIGN

*A case study in interface verification.* Symbios Logic uses top-down timing design to ensure proper interfaces in a multi-time-domain ASIC. Kurt Kastein, Symbios; Mike McClure, Chronology; *Integrated System Design*, 5/97, p. 19, 5 pp.

*Managing power in million-device IC design.* A complete system approach to microprocessor design includes power analysis. Ken Munson, Rise Technology; *Integrated System Design*, 5/97, p. 28, 4 pp.

## MEMORY

*New DRAMs aim to ease main-memory bottlenecks.* New interface standards, on-chip caches, and banked architectures all compete for places in future computation. David Bondurant, Enhanced Memory Systems; *Electronic Products*, 5/97, p. 63, 4 pp.

*Advanced DRAM architectures vie to succeed SDRAM.* As microprocessor speeds outpace DRAM access times, memory-chip makers are looking for new tricks. Faster choices like Rambus DRAM, SyncLink, and DDR DRAM jockey to succeed SDRAM. Jeff Child, *Computer Design*, 5/97, p. 65, 5 pp.

## MISCELLANEOUS

*Merging television with PCs—which display is in the picture?* The battle for the home-viewing audience continues as PC monitors compete with the sharpness and quality of TV screens. Eric Rayel, Rockwell; *Electronic Design*, 4/14/97, p. 141, 4 pp.

*Divide and conquer: binary division.* You can carry out binary division, one of the most difficult operations for a computer to perform, in simple µPs using low-level instructions. Clive Maxfield, Intergraph; *EDN*, 5/8/97, p. 163, 3 pp.

## PROCESSORS

*Branch-effect reduction techniques.* This survey compares current hardware and software branch-effect reduction techniques, offering hope for greater gains. Augustus K. Uht, Univ. of Rhode Island; Vijay Sindagi, TI; *Computer*, 5/97, p. 71, 11 pp.

*Eight-bit microcontrollers grow up...and down.* They're acquiring capabilities that enable their inclusion in designs formerly handled by 4- or 16-bit devices. Rick Grehan, *Computer Design*, 5/97, p.72, 6 pp.

## PROGRAMMABLE LOGIC

*FPGAs take on the PCI performance challenge.* The latest-generation FPGAs have the density and performance to handle the speed and complexity of PCI. Dave Bursky, *Electronic Design*, 4/14/97, p. 111, 6 pp.

*FPGA design practices that help ensure good migration.* Migrating a design between an ASIC and an FPGA requires special consideration of some design issues. Ron Modo, Lucent; *Integrated System Design*, 5/97, p. 42, 4 pp.

## SYSTEM DESIGN

*Display-works conference spotlights U.S. manufacturing advances.* Advanced R&D funding in materials and tools allows domestic display makers to catch up with the competition. Cheryl Ajluni, *Electronic Design*, 4/14/97, p. 55, 3 pp.

*Lilliputian passives herald hybridlike PC-board density.* In microscopic form factors, components, arrays, and networks—both resistive and reactive—allow unprecedented board density. Bill Travis, *EDN*, 5/8/97, p. 111, 5 pp.

*Engineers lay out virtual PC boards at earliest design stage.* Once engineers could confidently throw a design "over the wall" to a PC-board designer for layout. Now they must begin layout of virtual PC boards themselves at the start of the design process. Charles H. Small, *Computer Design*, 5/97, p. 50, 4 pp.

*Consider emerging standards when selecting IP.* You won't achieve the productivity increase you need for system-on-a-chip design without design reuse. You must maintain up-to-the-minute awareness of emerging technical standards for IP-based design. Barbara Tuck, *Computer Design*, 5/97, p. 56, 4 pp.