SGS-Thomson Raises Metaflow Stake

In a move that could make it a more significant player in the x86 market, SGS-Thomson (ST) has acquired Hyundai's interest in processor design house Metaflow Technologies *(www.metaflow.com)*, making ST the majority owner. Metaflow, headed by president Val Popescu and lead architect Bruce Lightner, has developed a series of advanced, out-of-order processors during the past decade. Previous designs, none of which ever went into production, were all multichip SPARC implementations: first an ECL design; then a CMOS processor, called Lightning, created for LSI Logic (see MPR 9/19/90, p. 4); followed inevitably by Thunder, developed for Hyundai (see MPR 8/22/94, p. 4).

Metaflow's pioneering efforts in out-of-order processor design have since been validated, as nearly every high-end CPU vendor has adopted this technique. The Thunder design, which required three chips in 0.8-micron technology, could easily be placed on a single 0.35-micron chip. By coupling this superscalar RISC engine with an x86 front end, Metaflow could produce a chip similar to Intel's P6.

Piero Martinotti, VP of SGS-Thomson's New Ventures Group, acknowledged that Metaflow is working on an x86 processor design but said the primary goal is to provide building blocks for "superintegration" ASIC products. ST currently has a Cyrix-derived 486 core available as part of this program. The high-end performance point that has been Metaflow's focus seems an ill fit for ASICs, however, and the superintegration plan may be a cover story for an effort to go after the mainstream PC microprocessor market.

ST has an Intel patent license, acquired along with Mostek many years ago, that the company has used to produce Cyrix-designed processors. The Cyrix agreement has strict limits on the number of chips ST can sell under its own name, however, and ST never produced volumes of the 6x86 for Cyrix. ST has suffered from Cyrix's focus on IBM's process technology, which made it hard to produce the 6x86 in ST's fabs. The Metaflow acquisition could indicate a shift in ST's x86 strategy toward in-house designs. —*M.S.*

Motorola Extends 860 Line at Top, Bottom

Two new low-cost versions of Motorola's popular but expensive MPC860 communications processor lower prices to below $30, and a new high-end version extends the company's PowerQUICC line with ATM support.

The new MPC850 and 850SE are both functional subsets of the half-dozen PowerPC-based MPC860 devices already in Motorola's product line (see MPR 9/11/95, p. 9). The 850SE eliminates three of the 860's four serial-communications controller (SCC) channels, including all protocols except Ethernet, and more than half of the cache. The resulting chip has 2K/1K instruction/data caches, a DMA controller, and one Ethernet channel. The 850 upgrades the lone SCC channel with HDLC and other protocols and adds a USB port. The two chips are pin-compatible; both are housed in a 256-contact ball-grid array. In 10,000-unit quantities, prices for the 850SE and 850 start at $27 and $29, respectively. Production begins in 3Q97.

The MPC860SAR throws in everything the other six 860-family devices already have and upgrades the four SCC channels with ATM segmentation and reassembly support (hence the product name). The laundry list of features includes a Utopia physical-layer (PHY) interface with multi-PHY support, transmission convergence for E1/T1, and support for constant and unspecified bit rates (CBR/UBR). The chip is intended for use in ADSL equipment, switches, and Ethernet-to-ATM interface units. The part lists for $61 in quantities of 10,000.

Motorola has played its communications card well for the past several years, parlaying its pile of intelligent peripherals and CPU cores into a full house of communications-related microprocessors. The MPC860, the first PowerQUICC, added a PowerPC core to the earlier 68360 (see MPR 5/10/93, p. 13). To date, most of Motorola's embedded PowerPC sales come from this line. With lots of first-hand information on communications infrastructure and plenty of I/O and CPU options to draw from, Motorola has consistently been QUICC on the draw. —*J.T.*

LSI Logic Develops Digital-Camera Chip

LSI Logic's new DCAM-101 device combines a MIPS processor core with several custom-developed logic blocks to create a single-chip controller for digital still cameras. Priced at $35 in "high volume," the device includes nearly everything required except the memory, lens, CCD, and LCD display.

Packed into the DCAM-101's 256-lead TQFP package are a 54-MHz CW4010 MIPS core (see MPR 12/26/94, p. 15), a 2K instruction cache, a 256-byte data cache, 2K of SRAM, a pixel interpolator with a 32 × 32-bit hardware MAC, PC Card interface, JPEG codec, DMA controller, and 8-bit LCD display controller. LSI claims a compression rate of 3.3 million pixels/s, fast enough to capture 11 true-color 640 × 480 images per second; at the chip's maximum 2,048 × 2,048 resolution, compression takes 1.2 seconds per frame.

Although the part consumes a hefty 1.2 W running at full speed, in normal operation the chip spends most of its time in one of several power-saving modes. Viewfinder mode maps the incoming image to the LCD display in real time. Capture mode compresses the incoming image and stores it to external memory. Recall mode reverses the process, retrieving compressed images and displaying them on the LCD or an external monitor. An on-chip NTSC/PAL encoder allows images to be viewed on a TV; a serial interface can be used to download compressed images to a PC for archiving, transmission, or display.

In all, the DCAM-101 provides most of the features one could want for a digital-camera controller. LSI also provides a development board with software for prototyping. This is LSI's first foray into digital cameras; Fujitsu and Motorola have both been successful here with SPARClite and PowerPC 821 chips, although neither of these chips is as highly integrated as the DCAM-101. We expect this segment of the consumer-electronics market to boom for several years as the quality of digitally captured images and inexpensive ink-jet printers both improve. With their combined emphasis on low cost, small size, long battery life, and high resolution, these cameras will provide a design challenge for any vendor with its eye on the digital-camera market. —*J.T.*

Trident, NeoMagic Combine Graphics, DRAM

NeoMagic, the first vendor to introduce a graphics accelerator with an integrated frame buffer (see MPR 3/6/95, p. 20), continues to enhance its product line, but the startup faces new competition from Trident Microsystems (*www.trid.com*). Trident's new Cyber9388 combines the 3D core from the company's 3DImàge family (see MPR 6/2/97, p. 16) with 2M of embedded DRAM. Trident's chip is built in Samsung's 0.35-micron CMOS merged-DRAM technology.

The Cyber9388 adds dual-display support, driving up to two display devices, including dual-scan and TFT LCDs, standard RGB monitors, and NTSC/PAL televisions. Video playback is enhanced by a filter circuit that reduces flickering in interlaced displays like televisions. The chip also handles color-space conversion and smooth rescaling to any screen resolution.

The Cyber9388 includes a "universal" 32-bit PCI interface that supports 33-MHz and 66-MHz clock rates plus 3.3-V and 5-V signaling, making it suitable for virtually any of today's notebook designs. The Cyber9388 is priced at $45, with volume production scheduled for 3Q97.

Not standing still, NeoMagic has introduced its fourth-generation chip, the MagicGraph 128XD, which is already in volume production. It is fully PC 97–compliant and supports 1,024 × 768 × 16 LCDs. Like the Trident chip, the 128XD has an NTSC/PAL video output with flicker filtering. The 128XD's LCD drivers include the vendor's MagicPass EMI-reduction technology, reducing one of the most significant problems facing notebook-computer vendors.

NeoMagic touts the 128XD as a 3D accelerator, but in truth the part does not include a 3D-rendering engine; the claim is based solely on features that speed MMX-based software 3D rendering, such as support for Direct3D-style frame buffers with interleaved color and Z values. Trident's part, with a megatriangle 3D engine, will offer much better 3D performance than NeoMagic's device.

Both integrated graphics chips offer significantly reduced power and board-space requirements compared with traditional designs, which require two or four external DRAMs. NeoMagic quotes the 128XD's power consumption at less than 0.5 W (typical). This is only 20% of the power consumed by traditional designs. Board space is similarly reduced from about four square inches to only one.

NeoMagic (*www.neomagic.com*) has not announced pricing but says the 128XD is priced competitively against traditional designs, after accounting for the external DRAM and extra board space required for such solutions.

With its early delivery of several graphics accelerators with integrated frame buffers, NeoMagic has secured design wins with many major notebook vendors, leading to a recent successful IPO. But now that Trident has adopted the same technique, and with others likely to follow, the established vendor will have to compete on features and price. Trident's chip packs 3D performance, but we believe the NeoMagic chip costs less and requires less power, giving it an advantage for systems in which 3D is not a requirement. —*P.N.G.*

250-MHz 604e Chips Trickle Into Market

Renegade Macintosh system maker Power Computing *(www.powercc.com)* rolled out what it claims to be the world's fastest personal computer, based on a 250-MHz PowerPC 604e processor from IBM. The PowerTower Pro 250 is available now at a base price of $4,495, which includes 1M of L2 cache, 32M of memory, a 2G hard drive, 16× CD-ROM, and an 8M graphics card.

Power Computing is obtaining the fast chips from IBM, which has not officially announced pricing or general availability of the parts. The new parts use the same IC process as the company's 233-MHz 604e (see MPR 4/21/97, p. 1), but apparently the speed yields are not yet good enough to produce 250-MHz chips in volume.

Power's performance claim is based on IBM's estimated SPECint95 rating for the 604e-250, which exceeds the score of a Pentium II-266. IBM's estimate, however, assumes future compiler and system enhancements; based on published numbers for current 233-MHz 604e systems, we estimate the PowerTower Pro 250 could deliver 9.0 SPECint95 (base), significantly less than the 10.4 SPECint95 (base) measured on a 266-MHz Pentium II system. PowerPC continues to underdeliver on its performance promises. —*L.G.*

Windows CE Running on NEC's R4300

NEC has announced immediate availability of Windows CE for its R4300 microprocessor, making it the fastest CPU announced so far to run the new operating system. The chip required no modifications for CE; its MMU is a superset of that on the R4100 series. Microsoft's initial focus, however, was on low-power devices for handheld PCs. Thus, the R4101 was NEC's first to host the new OS. —*J.T.*

Erratum: ATI Perspective Correction

In our previous issue (see MPR 6/2/97, p. 16), we incorrectly reported that ATI's Rage Pro uses quadratic approximations for texture perspective correction. While previous ATI 3D chips used this technique, the Rage Pro implements true perspective correction with a per-pixel divide algorithm. M