by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send e-mail to belgard@umunhum.stanford.edu *with comments or questions.*

5,603,047

Superscalar microprocessor architecture
Issued: February 11, 1997
Inventor: Robert L. Caulk, Jr.
Assignee: LSI Logic
Filed: October 6, 1995
Claims: 10
A RISC microprocessor core with a dual six-stage pipeline, each pipeline having instruction-fetch, conditional queuing, decode/read, execution, cache read for load-and-store instructions, and write-back stages.

5,603,045

Microprocessor system having instruction cache with reserved branch-target section
Issued: February 11, 1997
Inventor: Kenneth A. Dockser
Assignee: VLSI Technology
Filed: December 16, 1994
Claims: 3
An instruction cache separated into a branch-target section and another section in which the branch-target section is updated with the target on a branch taken and the other section is updated on a branch not taken.

5,603,037

Clock disable circuit for translation buffer
Issued: February 11, 1997
Inventor: Husnu G. Aybay
Assignee: Intel
Filed: April 23, 1993
Claims: 21
A system for saving power in a microprocessor in which the TLB of a segmented and paged microprocessor is powered off either when paging is disabled or when paging is not disabled but address translation is not occurring.

5,600,848

Counterflow pipeline processor with instructions flowing in a first direction and instruction results flowing in the reverse direction
Issued: February 4, 1997
Inventors: Robert F. Sproull, et al
Assignee: Sun Microsystems
Filed: June 7, 1995
Claims: 60
A general-purpose computer in which instructions flow one way through the pipeline and results flow the other way, similar to a dataflow machine.

5,600,845

Integrated-circuit computing device comprising a dynamically configurable gate array having a microprocessor and reconfigurable instruction-execution means and method therefor
Issued: February 4, 1997
Inventor: Kent L. Gilson
Assignee: Metalithic Systems
Filed: July 27, 1994
Claims: 18
An FPGA is configured to implement a RISC processor. The execution unit is dynamically reconfigured to implement new instructions in hardware.

5,600,837

Multitask processor architecture having a plurality of instruction pointers
Issued: February 4, 1997
Inventor: Alain Artieri
Assignee: SGS-Thomson
Filed: May 24, 1994
Claims: 17
A multithreaded processor architecture is given. The architecture includes multiple instruction pointers associated with multiple tasks, a priority mechanism to allocate a priority to the tasks, and a task scheduler for scheduling the tasks on the processor.

5,600,806

Method and apparatus for aligning an instruction boundary in variable-length macroinstructions with an instruction buffer
Issued: February 4, 1997
Inventors: Gary L. Brown, et al
Assignee: Intel
Filed: March 1, 1994
Claims: 7
The circuit and methods of the Pentium Pro instruction buffer and portions of the decoder are claimed. The disclosure shows how the variable-length Intel instruction set is packed into the instruction buffer to ensure that the buffer contains full instructions for the decoder.

OTHER ISSUED PATENTS

5,603,041 *Method and system for reading from an m-byte memory utilizing a processor having an n-byte data bus*
5,603,017 *Parallel integrated circuit having DSP module and CPU core operable for switching between two independent asynchronous clock sources while the system continues executing instructions* ▣