SGI Updates MIPS Roadmap

Just three months after issuing a new roadmap (see MPR 5/12/97, p. 14), Silicon Graphics has changed it plans, extending its R12000 line and killing its Beast program. SGI now believes the R12000, which recently taped out, has more performance scalability than it previously anticipated. At the same time, the Beast program, which had already slipped a year from its initial schedule, was becoming unwieldy and had the potential for further schedule delays. MIPS President John Burgoin, who took over the top spot just nine months ago, pulled the trigger.

The company still expects the R12000 to begin volume shipments in 1H98 but now believes the part will reach clock speeds in excess of 300 MHz using the initial 0.25-micron process. The new roadmap shows R12000 clock speeds continuing to increase using more advanced manufacturing processes; SGI plans to take the chip all the way down to a true 0.18-micron process. We expect this latter version to appear in 1999 at clock speeds of up to 450 MHz.

We estimate that the initial R12000 should deliver close to 20 SPECint95 (base) and almost 30 SPECfp95 (base). The 450-MHz version could push these scores to 30 and 45. SGI says Beast would have delivered about the same scores but with more design effort and a higher chip cost. Staying with the R12000 design through 1999 also allows pin-compatible upgrades and averts the need to reoptimize application binaries for a new CPU core.

The downside of the switch is a huge reduction in bandwidth. Beast was designed to deliver 5 Gbytes/s to main memory. The R12000, in contrast, retains the same bus as the R10000; if the clock speed of this bus can be improved from 80 MHz to 200 MHz (a daunting task), it would still deliver less than a third of Beast's bandwidth. Even with larger L2 caches, this difference could have a significant impact on the large scientific and transaction-processing applications that SGI is now focusing on. By 1999, the company may revise the R12000's bus interface to ease this bottleneck.

Because advancing the R12000 will require far fewer engineers than finishing Beast, SGI has redeployed most of the Beast designers to the H2 processor. With the extra staff, the H2 is now poised to debut in 2000 instead of 2001. In addition, SGI has significantly increased its performance target for the H2, due to some improvements in the design.

In the short term, we expect to see 0.25-micron versions of the R10000 running at up to 275 MHz by the end of this year. These parts will continue as lower-cost options to the R12000 after that device is released.

While it is always painful to kill a project, in this case SGI has simplified its product offerings while accelerating its next-generation program. The key question is whether the revamped R12000 can be competitive in 1999 against Intel's Merced and other newer designs. —*L.G.*

Intel Halves Prices on Most Chips

As we reported in our last issue (see MPR 7/14/97, p. 1), Intel's third-quarter prices, officially announced on July 28, are about 50% lower than the previous quarter's prices for both the MMX and non-MMX Pentium processors. The new prices (see MPR 8/4/97, p. 27) revalue the Pentium chips to reflect the nearly nonexistent demand for the non-MMX versions. In fact, Intel confirmed that it is no longer starting wafers of the old P54C design, meaning that shipments will cease sometime in the fourth quarter.

The low-end Pentium/MMX chip for the desktop, the P55C-166, is now at a 1,000-piece list price of $145, making it suitable for PCs well below $1,500. Only the relatively new P55C-233 escaped a 50% price cut; at $386, the chip now sells for 35% less than its introductory price.

On the mobile side, the cuts were a bit less severe. The low-end MMX chip, in this case the P55C-133, sank 38% to $177, but the faster versions of the Mobile Pentium/MMX processor fell less than 30%. The fastest mobile part, the P55C-166, is now at $348, leaving room at the top of the line for the imminent release of the mobile P55C-200 and -233 parts, code-named Tillamook.

Because Intel is constrained in its ability to ramp production of the larger Pentium II processor, prices for these chips did not fall at the same rate. The 233- and 266-MHz versions received price cuts of only about 15%, small even for a more normal Intel quarter. Look for more aggressive price cuts for Pentium II in future quarters as Intel's factory constraints are eased and it looks to move the new processor into the volume segments of the PC market.

The biggest change in Pentium II pricing is for the 300-MHz version, which fell all the way from $1,981 to $851 before it even started shipping in volume. Intel originally positioned this part for workstations only (see MPR 5/12/97, p. 1), as yields at this speed were expected to be very small. Initial production of Pentium II has generated better volumes at this speed, and Intel now believes the 300-MHz part will be part of its PC offerings from the 0.28-micron process. A move to 0.25-micron Pentium II chips, due in early 1998, will ultimately produce speeds in excess of 400 MHz. —*L.G.*

Sony, Hyundai Take Up ARM Licenses

Amazingly, Advanced RISC Machines (ARM) discovered two semiconductor vendors that were not already licensees of its technology. The two newest inductees are Hyundai Electronics Industries and Sony. The publicly acknowledged membership in this august body now stands at 21.

Both companies licensed the ARM7TDMI core, which includes a hardware multiplier, debug interface, in-circuit emulator tap, and the Thumb code-compression module (see MPR 3/27/95, p. 1). Sony additionally licensed the

semistandard AMBA (advanced microcontroller bus architecture) internal bus interface with peripherals, along with an option for future CPU core designs.

Regarding its product plans, Sony says only that it intends to use ARM cores in future consumer and professional electronics products (which pretty much covers Sony's entire product line). Following a well-worn path, Hyundai plans to develop cellular communications devices, specifically CDMA/PCS applications, using ARM. —*J.T.*

Hitachi Does SH7709, Core-Logic Pair for CE

Hitachi is sampling its upgraded SH7709 microprocessor along with a companion chip that together make a complete chip set suitable for Windows CE–based handheld devices. The pair sells for $70 in sample quantities; production pricing has not been released.

The SH7709 is a faster version of the SH7708 (see MPR 3/6/95, p. 12) that runs at 80 MHz, 33% faster than the 7708. The new chip also has a DMA controller, 10-bit A/D and 8-bit D/A converters, and three serial channels that the older chip does not. The new HD64461 companion chip provides a color LCD controller, a combination PC Card and Mini Card interface, an I^2C interface, a 4-Mbps IrDA interface, interrupt control, power management, and an analog front end for a software modem.

The new chip set is similar in feature set to the SH7707 processor used in HP's palmtop PC, the 320LX, except that the 7707 handles only grayscale LCD screens. Hitachi has not, however, made the 7707 generally available. The color LCD controller on the 64461 delivers 640 × 480 × 8-bit (256-color) resolution, which will be an attractive upgrade feature when Microsoft releases the next version of Windows CE, which supports color displays.

At $70, the Hitachi pair is considerably more expensive than Philips's two-chip set for WinCE, the 31700/UCB1200. The Dutch company charges just $39 for its set, which has most of the same features as Hitachi's except for the PC Card/Mini Card interface. The 75-MHz MIPS core in the 31700 should yield about the same performance as the 80-MHz SuperH chip, and both have similar power requirements: just under 300 mW. Unless the SH7709's memory-card interface or better code density are important, Philips's 31700 seems the better bargain. —*J.T.*

Siemens Nabs Java for Smart Cards

Sun and Siemens have signed an agreement that allows the German technology giant to develop new "smart cards" that execute Java bytecode. Development of the new smart-card processor has just begun; samples are expected early in 1998, with production by the middle of that year.

The new processor core is a proprietary Siemens development. Instead of using Sun's PicoJava core (see MPR 10/28/96, p. 28), the tiny CPU will be based on Siemens' recently introduced SLE66 "Triple-E" line of embedded 16-bit microprocessors. The '66 instruction set is a superset

Letters to the Editor

A response to Michael Slater's column, Waiting for Microsoft *(see MPR 5/12/97, p. 19):*

Microsoft does not get the majority of its operating system revenue from selling to the installed base; the majority comes from new PC and server purchases. Microsoft's principles of backward compatibility and support of the installed base are based on customer input. Last year, we made an OS release that focused only on new hardware features and was sold only with new computers (the Windows 95 OSR2 release). Customers and software developers told us that they prefer a release that is available as a retail upgrade as well as for new machines. For customers, it represents lower cost of training and support to use the same OS release; for software developers, it means that they can leverage their development and testing efforts over a larger base of customers.

Providing support for new hardware standards represents a special challenge. Frequently, early implementations have a long list of errata, which we help to find; until the hardware is reasonably stable, software development and debugging cannot be completed. This is then followed by internal testing and beta testing. Our experience has been that early support that is too narrow or has too many incompatibilities or bugs does not result in market adoption. At best, support for new hardware standards cannot ship in an OS release until six months after production-quality hardware and peripherals are available for the test process.

Ultimately there are multiple constituencies for an OS release, and they have differing, often conflicting requirements. Hardware makers want timely support of new hardware features. Software developers want a consistent platform and support for the latest APIs. The Internet has rapidly evolving standards. Yet both business and consumer end users want a high-quality, robust, stable release, and they will trade a time delay or feature reduction for stability. We try hard to make a reasonable compromise among these requirements.

Many exciting technologies are supported in the next releases of Windows 95 and Windows NT, including DVD, AGP, ACPI, and OnNow, as well as a rich set of USB peripherals. We are hard at work developing and testing this support, knowing that the industry wants this support to ship as soon as possible. We are focused on achieving that while also providing the level of testing and quality that ensures rapid customer adoption and minimum end-user support costs, so we create the largest possible market for the new hardware.

If you have suggestions for how to manage the priorities differently, I am eager to hear them.

—Carl Stork, General Manager, Microsoft

of the venerable 8051 architecture, which Siemens extended for use in smart-card controllers. The planned Java-enabled chips will layer still more features on top of the '66 CPU core.

The resulting CPU will be "bilingual," executing either 8051 code or Java bytecode. It will not execute the entire Java instruction set, as PicoJava attempts to do, but rather a minimal subset of bytecodes that Sun has dubbed JavaCard. Unlike PicoJava, the Siemens core will execute all JavaCard instructions in hardware, with no software overhead or emulation.

Siemens is already a major vendor of microcontrollers for smart cards, which are far more popular in Europe than in North America. Today, most such controllers are based on 8- or 16-bit CPUs, with a few kilobytes of nonvolatile memory. Siemens and Sun are banking on the JavaCard API to fuel a new range of applications in banking, health care, wireless telecommunications, and electronic commerce. —*J.T.*

Toshiba Rolls Out First MIPS-16 Chip

Toshiba's TMP1904AF is the company's first chip to use the new MIPS-16 code-compression option (see MPR 10/28/96, p. 40) and only its second significant MIPS product in as many years. The part is initially priced at $17.50 (in 10,000-unit quantities) and begins sampling in December. Production is scheduled for 1Q98.

The 1904 includes a moderate amount of integration. In addition to its 32-bit R3000 core and 4K/1K instruction/data caches, the chip includes 1K of SRAM, a DRAM controller, a two-channel DMA controller, two serial ports, timers, and debug logic. The device is housed in a PQFP-160 package and runs from a 3.3-V supply.

Power consumption is a mere 35 mW (typical), according to Toshiba. According to the company, part of this low dissipation is due to the 1904's lackadaisical 20-MHz clock rate and part is due to low-power design techniques. Toshiba expects to increase the clock rate after further testing and a move to 0.25-micron CMOS in 1998. The new process is also tailored to take advantage of Toshiba's merged DRAM/logic design (see MPR 8/4/97, p. 19).

Although several processors offer better performance than the 1904 at a lower price, few can match the Toshiba chip's impressively low power rating. IBM's 401GF sells for just $11 and can be clocked at 25 MHz, bringing its power consumption down to 40 mW. That chip, however, doesn't have the 1904's integrated logic. Other 32-bit processors generally require at least 100 mW.

Thus, the 1904 is well suited for portable devices that have tight power and cost budgets and need 32-bit performance. The chip's integrated system logic will reduce the burden on external ASICs, and its code compression will minimize the amount of external memory needed. It is likely to appear in high-end organizers, cellular telephones, and other handheld devices. —*J.T.*