by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send e-mail to belgard@umunhum.stanford.edu *with comments or questions.*

5,606,682

Data processor with branch-target address cache and subroutine return-address cache and method of operation
Issued: February 25, 1997
Inventor: Ralph C. McGarity
Assignee: Motorola
Filed: April 7, 1995
Claims: 7
A processor with a call/return-address cache and a branch-target cache for storing a number of recently encountered fetch address-target address pairs.

5,606,676

Branch-prediction and resolution apparatus for a superscalar computer processor
Issued: February 25, 1997
Inventors: Edward T. Grochowski, et al
Assignee: Intel
Filed: February 9, 1995
Claims: 13
A circuit for predicting a branch target, comprising two pipelines for processing instructions, a decoder with logic to associate the branch to one of the two pipelines, and a branch-target buffer.

5,606,675

Data processor for invalidating prefetched instruction or branch-history information
Issued: February 25, 1997
Inventors: Ken Sakamura, et al
Assignee: Mitsubishi
Filed: April 21, 1994
Claims: 7
An instruction-cache invalidate instruction is provided. The invention requires that this instruction be executable by a user program to invalidate its instructions from the cache.

5,606,670

Method and apparatus for signaling a store buffer to output buffered store data for a load operation on an out-of-order-execution computer system
Issued: February 25, 1997
Inventors: Jeffrey M. Abramson, et al
Assignee: Intel
Filed: April 22, 1996
Claims: 32
Store-forwarding circuitry in an out-of-order processor having a store buffer of buffered memory-store operations. The circuitry conditionally forwards "store" data for a memory-load operation from a subset of the buffered memory-store operations to subsequent load operations.

5,604,909

Apparatus for processing instructions in a computing system
Issued: February 18, 1997
Inventors: Chandra Joshi, et al
Assignee: Silicon Graphics
Filed: December 15, 1993
Claims: 19
A two-level instruction buffer that may dispatch multiple instructions in parallel from the first level, then refill the first level from instructions in the second level.

5,604,905

Method and apparatus for architecture-independent executable files
Issued: February 18, 1997
Inventors: Avadis Tevanian, et al
Assignee: Next
Filed: February 28, 1995
Claims: 20
A method and apparatus enabling a single release of software for multiple architectures and operating systems. The invention provides a single file that contains separate object code for each of multiple architectures, with a special header that identifies each section of object code and includes pointers to its starting location.

5,604,877

Method and apparatus for resolving return-from-subroutine instructions in a computer processor
Issued: February 18, 1997
Inventors: Bradley D. Hoyt, et al
Assignee: Intel
Filed: January 4, 1994
Claims: 28
Method and apparatus for resolving return-from-subroutine instructions in a computer processor. A first stage predicts call and return instructions, storing a return address in a register. The register forms a predicted top-of-return-address stack, which is pushed, if the prediction is correct, or discarded.

OTHER ISSUED PATENTS

5,606,714 *Integrated data-processing system including CPU core and parallel, independently operating DSP module, and multiple operating modes*
5,604,878 *Method and apparatus for avoiding write-back conflicts between execution units sharing a common write-back path*
5,604,689 *Arithmetic-logic unit with zero-result prediction* ■