Tillamook Debuts at 233 MHz

The first product off Intel's new 0.25-micron line is a processor for notebooks, not desktop systems. The new technology allows Intel to extend its Mobile Pentium/MMX line from 166 to 233 MHz with a product code-named Tillamook (see MPR 1/27/97, p. 4). From a functional standpoint, the new part is identical to existing Mobile Pentium/MMX chips.

A key advantage to the 0.25-micron technology is its ability to operate at low voltages. Tillamook uses a core CPU voltage of 1.8 V, compared with 2.45 V for the P55C-based Mobile Pentium/MMX parts. In addition, the I/O voltage is reduced from 3.3 V to 2.5 V. Intel's 430TX chip set is the only one that supports a 2.5-V processor bus, but other vendors are likely to adapt their notebook chip sets to this voltage soon. SRAMs that operate at 2.5 V are now available from a number of suppliers.

Due to the lower voltages, Tillamook consumes about 60% less power than the Mobile P55C at the same clock speed. Even at 233 MHz, Tillamook has a typical power dissipation of 3.9 W, compared with 7.2 W for the 166-MHz Mobile P55C. Tillamook clearly has headroom to reach 266 MHz, if Intel chooses to extend this line.

Tillamook's lower power extends the battery life of notebook PCs even as their CPU performance improves. Lower power also eases thermal problems for notebook designers, who have been stressed by the power level of the P55C parts. Like its predecessors, Tillamook will be sold either alone in a 320-lead TCP package or as part of a Mobile Module (see MPR 2/17/97, p. 9).

For the dual benefits of low power and high performance, Intel is charging a stiff premium: $530 for the 200-MHz version, $691 for the top-of-the-line part. (Add $74 to get the part mounted on a module with 512K of cache and the 430TX north bridge.) By comparison, a 166-MHz Mobile P55C lists for just $348. The 233-MHz Tillamook costs nearly twice as much as the 233-MHz desktop version. At these prices, we expect Tillamook will appear only in premium notebook systems, at least until a scheduled price cut in November.

Intel will cut Tillamook's price rapidly during 1998 as faster Mobile Deschutes parts appear. The 0.25-micron process reduces Tillamook's die size to 95 mm^2, bringing its estimated manufacturing cost to $40. Thus, the company has plenty of margin to absorb future price cuts. In the meantime, Tillamook will be Intel's highest-margin processor.

It's unusual for Intel (or any other CPU maker) to devote a new IC process to a product other than a high-end desktop processor. The low voltage of the 0.25-micron process is particularly well suited for mobile processors, but choosing this target locks out three-quarters of the total market, reducing demand for the new device. Tillamook's excessive profitability may have influenced the decision, but Intel really had no choice in the matter: Deschutes, the 0.25-micron desktop product, wasn't ready in time to be the lead product off the line. Watch for Deschutes (see MPR 8/25/97, p. 10) to debut early next year. —*L.G.*

Motorola Previews New M•Core Architecture

Compulsive processor designer Motorola has created yet another new 32-bit microprocessor architecture, this one aimed at portable consumer electronics. Dubbed M•Core, the new architecture is designed to be smaller and more power-efficient than anything Motorola currently has in its arsenal. Although the technical details of M•Core will not be released until October's Microprocessor Forum, the company did preview its goals for the new line.

M•Core is expected to address the gap in Motorola's product line between PowerPC (high end) and ColdFire/68K (low end) for low-power chips. The company is initially targeting digital wireless communications (cell phones and pagers) and portable systems. The M•Core CPU core will be used in application-specific devices from Motorola and will appear in its FlexCore ASIC library for user designs. In a significant break from tradition, Motorola also plans to license M•Core to outside vendors, à la ARM and MIPS. Given the large number of current ARM and MIPS licensees, however, it isn't clear which CPU makers might be interested in an M•Core license.

Motorola claims the first M•Core devices, due in 2Q98, will run at about 50 MHz in Motorola's 0.35-micron process. Supply voltages range from 3.3 V down to 1.8 V, with clock speed decreasing with voltage. Unlike current ColdFire or embedded PowerPC chips, M•Core will use leading-edge IC processes to save power. Motorola's roadmap calls for process changes at 18-month intervals, moving to 0.20 microns in early 1999 and 0.15 microns in 2000. By that time, supply voltages should be below 1.0 V.

M•Core is positioned to compete with MIPS, ARM, and other licensed CPU cores in the burgeoning market for portable computing and communications devices—markets in which Motorola products are dominant, but its microprocessors are not. According to the company, M•Core is 25% to 400% faster than ARM7 on a number of C benchmarks while providing an average of 50% better code density (10% better than ARM7/Thumb).

It may be late in the game to be introducing an entirely new 32-bit architecture, but that has not discouraged Motorola or a number of other vendors eyeing the booming portable-electronics market. There are not yet any dominant architectures in this market, though ARM has an early lead with digital cell-phone makers. Even with all its CPU lines, Motorola has no appropriate technology in the low-power 32-bit arena. Rather than license MIPS or ARM (as its cellular products group did; see MPR 3/31/97, p. 4), the semi-

conductor group chose to develop something from the ground up. At the very least, M•Core is likely to appear in several Motorola consumer products by the end of the decade; for most vendors, that would be reason enough to develop a new instruction set. —*J.T.*

Apple Kills CHRP, Clone Market

Reversing course, Apple has essentially pulled the plug on the Mac clone market. Despite operating without a titular CEO, within the space of a few weeks the company (1) said it would not support Mac OS on CHRP systems, (2) denied its licensees access to the recently released Mac OS version 8.0, and (3) purchased for $100 million the Macintosh license and all other Mac-related assets of Power Computing, the largest of the clone vendors.

CHRP was originally intended as a common platform for systems running Windows NT, OS/2, Unix, and Mac OS (see MPR 12/5/94, p. 8). As PowerPC support for these various operating systems fell by the wayside, CHRP became the "open" platform for the Mac clone makers, which otherwise were restricted to using Apple's own ASICs. But more than 30 months elapsed between the announcement of CHRP and the availability of the first CHRP systems, and by that time Apple had changed its mind about allowing competition in the Mac market.

Both Motorola and VLSI had developed system-logic chip sets for CHRP, but with Apple sticking to its own ASICs, these products now have no customers. Power Computing is now just another PC maker, and at press time, the other two Mac licensees—Umax and Motorola—were twisting in the wind while Apple decided their fate. The great dream of PowerPC has vanished, leaving Apple and IBM as the only vendors with a future in PowerPC systems. —*L.G.*

Sun, Acorn Push NC Reference Platforms

Sun Microsystems and Britain's Acorn Group (part owner of ARM) are both peddling their respective hardware designs as starter kits for makers of network computers. Sun has chosen to sell the actual hardware, while Acorn is giving the design files away to licensees of its NC operating system.

Sun's JavaEngine 1 is a 7" × 7" board with a 100-MHz MicroSparc-IIep (see MPR 5/6/96, p. 5), a graphics chip, an Ethernet controller, and miscellaneous I/O chips. With the addition of 16M of memory, the board is quite similar to the innards of Sun's JavaStation 1, which has been for sale since the beginning of this year. The $385 board comes with JavaOS and the Java Views user interface, but no additional software or applications. Sun offered no performance data for the board.

Acorn's design, which has been around for some time, was part of the reference platform for Oracle's NC. The board is based on a 40-MHz ARM7500FE running RISCOS, a scaled-down version of which became Oracle's NCOS. The Oracle/NCI "reference specification" for NCs, such as it is, mandates only that Java applications can be downloaded and run in some manner. As such, virtually any system (including PCs, Macintoshes, and most workstations) complies, although most early NC enthusiasm centered around ARM processors.

Sun and Acorn join National and IBM (see MPR 7/14/97, p. 5) in selling low-cost reference boards or giving away design files in order to spur interest in their processors or software. With NC design requirements fuzzy, and the potential market even fuzzier, it remains to be seen whether any of these designs reaches the mass market. —*J.T.*

AMD K6 Scores IBM Design Win

Gaining momentum, AMD's K6 will be used in some PCs in IBM's Aptiva line, marking the first top-tier design win for the K6. Digital was previously the largest PC maker to adopt the K6, although its motivation was probably rooted in its legal tussles with Intel (see MPR 6/2/97, p. 26). Interestingly, IBM PC Co. chose the K6 over the Cyrix-designed 6x86MX, which IBM Microelectronics manufactures and markets.

Although some manufacturing glitches slowed initial production, AMD says it will ship more than one million K6 chips in the third quarter and hopes to double that number in Q4. The company claims to have design wins at 8 of the top 20 PC makers, so supply, not demand, is currently the limiting factor for shipment volume.

Although the weak K5 caused AMD's market share to fall to roughly that of Cyrix, the larger company still had an advantage in its better access to the largest PC makers, most of which had been customers of AMD's 486. With a strong K6 product, these sales channels are beginning to pay off. Cyrix's 6x86MX, in contrast, has been successful only with smaller PC vendors. —*L.G.*

NEC V830R/AV Handles Real-Time MPEG-2

Building on its recently retooled V830 product line (see MPR 6/2/97, p. 22), NEC announced plans for a high-end part to do real-time decoding of MPEG-2 audio/video data streams without the help of a media accelerator. The V830R/AV isn't expected to begin sampling until mid-1998, but the company is already planning to use the part in DVD players, satellite decoders, and Internet terminals.

The new device will be two-way superscalar—a first for the V800 family—and run at 200 MHz, according to NEC. In addition to the V830's media-processing instructions, the V830R/AV adds a SIMD processor for full-speed MPEG-2 decoding. The chip will also have a Rambus interface, making it the first announced microcontroller to incorporate the high-speed memory logic.

Because the actual rollout of the chip is still a year off, NEC did not provide pricing, but the V830R/AV is expected to deliver 250 MIPS while consuming less than 2 W. The company is clearly determined to use the V800 family as a technology driver for a range of new media-aware consumer applications —*J.T.*