by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send e-mail to belgard@umunhum.stanford.edu *with comments or questions.*

5,617,554

Physical-address-size selection and page-size selection in an address translator
Issued: April 1, 1997
Inventors: Donald B. Alpert, et al
Assignee: Intel
Filed: December 23, 1994
Claims: 28
A processor (Pentium) implements a two-mode paging scheme for linear-to-physical address translation. In the first mode, page sizes are fixed to a single size. In the second mode, page sizes can be either of two sizes.

5,617,549

System and method for selecting and buffering even and odd instructions for simultaneous execution in a computer
Issued: April 1, 1997
Inventor: Eric DeLano
Assignee: Hewlett-Packard
Filed: August 26, 1994
Claims: 19
An instruction buffer bundles fixed-length instructions received from an instruction cache for simultaneous issue in a superscalar processor. A signal is generated by the instruction decoder if the instructions can be issued in parallel. If not, the buffer issues the first instruction and bundles the second instruction with the next instruction from the cache.

5,615,386

Computer architecture for reducing delays due to branch instructions
Issued: March 25, 1997
Inventors: Frederic C. Amerson, et al
Assignee: Hewlett-Packard
Filed: January 18, 1996
Claims: 9
A processor includes a prepare-to-branch instruction that can load the target of a subsequent branch instruction into the instruction cache in preparation for the branch.

5,615,350

Apparatus to dynamically control the out-of-order execution of load-store instructions in a processor capable of dispatching, issuing, and executing multiple instructions in a single processor cycle
Issued: March 25, 1997
Inventors: James H. Hesson, et al
Assignee: IBM
Filed: December 1, 1995
Claims: 4
In an out-of-order pipelined superscalar processor with a store-barrier cache, loads and stores are allowed to execute out of order except when the store-barrier cache predicts a store violation. In this case, the loads and stores are executed in order until the store instruction has been executed.

5,613,132

Integer and floating-point register-alias table within processor device
Issued: March 18, 1997
Inventors: David W. Clift, et al
Assignee: Intel
Filed: September 30, 1993
Claims: 30
In the P6 register-alias table, separate register-alias tables for floating-point and integer registers are renamed to a single reorder buffer in a superscalar microprocessor.

5,613,121

Method and system of generating combined storage references
Issued: March 18, 1997
Inventor: Robert J. Blainey
Assignee: IBM
Filed: October 19, 1994
Claims: 12
An apparatus and method for inspection of instructions within a predetermined instruction window determines if multiple loads and/or multiple stores can be combined to be replaced by multiple-load or multiple-store instructions.

5,613,083

Translation lookaside buffer that is nonblocking in response to a miss for use within a microprocessor capable of processing speculative instructions
Issued: March 18, 1997
Inventors: Andrew F. Glew, et al
Assignee: Intel
Filed: September 30, 1994
Claims: 30
The P6 TLB allows hit-under-miss to occur; that is, while a page-table walk is under way as the result of a previous miss, the TLB can be accessed for continuous hits.

OTHER ISSUED PATENTS

5,617,550 *Data processor generating jump-target address of a jump instruction in parallel with decoding of the instruction*
5,615,349 *Data-processing system capable of execution of plural instructions in parallel* M