With this issue, we inaugurate our expanded coverage of embedded microprocessors and have moved some items from Most Significant Bits to Embedded News. Full-length articles relating to embedded microprocessors are now designated by highlighted margins. We'd appreciate receiving your comments or impressions at editor@mdr.zd.com.

Motorola Spins Embedded 603e for $20

Motorola's new embedded variant of its PowerPC 603e slashes prices to nearly $20, signaling a strong move into the high-end embedded market. The new EC603e, shipping now, is identical to the existing 603e, but with the floating-point unit disabled.

The EC (for "embedded control") 603e comes in speeds of 100, 133, 166, and 200 MHz. In 10,000-piece quantities, the parts are priced at $20.69, $28.10, $35.91, and $44.50—an $8 spread between speed grades. These prices are about one-third the list price of the full-featured 603e used in Macintoshes. The EC parts are built on the same 0.5-micron and 0.35-micron fab lines as the desktop parts and are, in fact, the same devices but with the FPU disabled.

Apart from the FPU, the EC603e is compatible in every way with the desktop 603e (see MPR 2/16/95, p. 4). The part is available in either a 240-lead ceramic QFP or the standard 255-contact BGA package, which is compatible with current desktop processors, including the 603e, 604e, 740, and 750 parts. Like their desktop counterparts, the faster 166- and 200-MHz chips use split power supplies to accommodate their 2.5-V cores; all four versions use 3.3 V for I/O.

Motorola's new PowerPC parts are a terrific bargain. Digital's StrongArm-110 also runs at 200 MHz and sells for about $45, but the ARM-based device does not offer the superscalar execution of the PowerPC. The SA-110 has the advantage of one-third lower power consumption, but this will be of interest only to makers of portable equipment. In Motorola's favor, the EC603e has a full-featured 64-bit system bus that handles multiple masters, split transactions, and cache snooping for memory consistency. Like Digital's SA-110, the EC603e's bus interface runs at a selectable fraction of the CPU core frequency.

With the fortunes of its desktop PowerPC business in disarray and its further participation in Somerset in doubt (see MPR 10/6/97, p. 3), Motorola is prudently making hay in embedded markets while the sun still shines on PowerPC. Although embedded sales currently account for only about 15% of PowerPC volume, that number will certainly increase, and Motorola is wise to position itself as a premier maker of embedded processors while the PowerPC franchise is still worth something. The EC603e makes a powerful price/performance argument for makers of high-end equipment with a need for high bus bandwidth, top integer performance, and good tool support. —*J.T.*

Intel Finally Ships i960HD, 'HT

After three years, Intel's long-awaited i960HD and i960HT have finally seen the light of day. The two new parts hold up the high end of Intel's aging 32-bit family, promising clock-doubled (for the 'HD) or clock-tripled ('HT) performance with a superscalar core. The 'HD runs at 80 MHz with a 40-MHz bus; the 'HT runs at 75 MHz with a 25-MHz bus.

The H-series chips in the i960 family (see MPR 10/3/94, p. 11) share a two-way superscalar core design and bus interface with the existing C-series parts but have larger caches and (now) higher clock rates. The 'HD and 'HT differ only in their internal clock multiplier (2× vs. 3×). Both provide a big performance increase over the 1× i960HA, which runs at 25, 33, and 40 MHz. With only 5 MHz separating their core clock rates, the performance of the 'HD and 'HT will depend mostly on their buses.

The 80/40-MHz 'HD is a logical upgrade for 40-MHz 'HA sockets, while the 75/25-MHz 'HT makes sense for 25-MHz 'HA designs. Even with its faster CPU, the slow bus on the 'HT will give it lower performance in most applications. In 10,000-unit quantities, the i960HD-80 is priced at $71.20 while the i960HT-75 lists for $68.75. For makers of laser printers and networking equipment based on the i960HA, these two parts will be a welcome upgrade. —*J.T.*

IDT's R4640 Reaches 180 MHz, WebTV Plus

Integrated Device Technology (IDT) has raised the speed of its 64-bit MIPS chip, the R4640, from 133 MHz to 180 MHz. The first announced customer for the newer speed grade is Microsoft's WebTV Plus home Internet receiver.

The R4640 now matches its bigger brother, the R4650 (see MPR 11/14/94, p. 18), in running at 133-, 150-, and 180-MHz clock rates. The two parts are identical except for the width of their external bus interfaces: 32 bits for the R4640 vs. 64 bits for the R4650. In quantities of 10,000, the R4640-180 is priced at $39; the 150-MHz version lists for $30. The R4650 carries a $30–$35 premium for the wider bus.

Although neither of these devices is very usable for portable systems, both are popular in networking and high-end printing applications due to their fast integer processing, single-precision floating-point units, and fast, wide bus interfaces. IDT has been something of a quiet force in the embedded MIPS market, yet the company has scored some high-profile design wins with WebTV, EchoStar/Dish Network, page printers, and numerous arcade games. The good floating-point performance, high bus bandwidth, and bargain prices of these devices may help IDT gain further recognition in the future. —*J.T.*

Sun Acquires Chorus Real-Time OS

Following its recent acquisition of Diba (see MPR 8/25/97, p. 4), Sun Microsystems is buying Chorus, the French real-

time operating-system vendor. The move gives Sun its first real-time OS and an entrée into telecommunications customers, where Chorus has been particularly successful. Sun also formed a new Embedded Systems Software Group with oversight of the company's three operating systems: Solaris, Chorus, and JavaOS.

Sun's need for a real-time OS is obvious, given the company's stated goal of becoming a major player in the embedded marketplace and the pronounced lack of such capability in either Solaris or JavaOS. Sun intends to maintain Chorus's current product line (including continued support of processors other than SPARC) and support its customer base. In the meantime, Sun will add elements of the Chorus operating system to future versions of JavaOS to give the latter a real-time flavor.

By bringing a capable real-time operating system on board, Sun is now much better positioned to make a legitimate attempt at penetrating the market for embedded systems. Its new access to telecommunications companies is especially important in light of Sun's belief that Java will become an important technology for such infrastructure companies. —*J.T.*

VLSI Glues ARM to Oak; ARM7 Hits 120 MHz

VLSI Technology has tweaked its ARM7TDMI core to reach speeds of up to 120 MHz in its 0.35-micron process—the fastest announced ARM7 core by far. Previous incarnations of ARM7 had generally been limited to half that speed. VLSI, however, has previously produced 66- and 80-MHz ARM7s. The company cites its long-term relationship with ARM (VLSI is an investor in Advanced RISC Machines), which allows VLSI to modify the basic ARM7 circuit design somewhat to shift critical paths and remove bottlenecks.

The company also announced a new design macro that combines the ARM7TDMI with the Oak DSP core, licensed from DSP Group (*www.dspg.com*). The two cores can be integrated into a single chip but operate independently, somewhat like Motorola's 68356 device. The V3670 evaluation chip, which combines these two cores with some memory and peripherals, is sampling now for $300 in single-unit quantities.

While VLSI is, like other companies, clearly yielding to the demand for mixed CPU/DSP devices (see earlier item), it's interesting that the company did not choose ARM's own Piccolo DSP extension (see MPR 11/18/96, p. 17). VLSI believes its customers want more performance than Piccolo can deliver. Whereas Piccolo and ARM7 are codependent, relying on each other for data and processing power, the Oak and ARM cores are independent—an arrangement that provides better overall performance, especially if DSP and control tasks must be accomplished simultaneously. The market demand for processors with DSP capability seems clear What is not yet clear is which approach—hybrid CPU/DSP or CPU and DSP together—will prevail. —*J.T.*

Siemens Reveals TriCore Plans

Siemens Microelectronics has begun providing the first hints of its new 32-bit embedded architecture called TriCore. Technical details will not be available until the Microprocessor Forum later this month, but initial indications are that TriCore will offer both control-oriented and digital-signal processing instructions within a single instruction set. The first TriCore parts are expected to ship in 2Q98.

The architecture, which was code-named Dolphin and then became Trillium before turning into TriCore, mixes DSP and conventional microprocessor features in a manner similar to Hitachi's SH-DSP or Motorola's M•Core (see MPR 9/15/97, p. 4). TriCore chips will use a mixed 16- and 32-bit instruction set; initial parts will allow two-way superscalar dispatch of instructions to multiple execution units. Two parallel 16×16-bit MACs, for example, will be supported, as will a number of SIMD operations on packed data. Speeds should be in the 100-MHz range. Circular and bit-reverse addressing modes are provided to aid DSP algorithms.

Siemens has developed a large and varied customer base over the years for its 8- and 16-bit microcontrollers, primarily in industrial and automotive markets. The company claims, for example, to offer 35 different varieties of the 8051 microcontroller. As controllers in automobiles, office equipment, and computer peripherals become more ubiquitous and more powerful, it was logical for the German Überfabrik to want a 32-bit upgrade path for its customers. Given its traditional customer base, a hybrid CPU/DSP architecture is a natural. By the time TriCore parts start appearing, Siemens will have its hands full competing against SuperH, M•Core, and Piccolo chips, all with variations on the now common CPU/DSP theme. —*J.T.*

Galileo Chip Set Adds 64-Bit PCI

Galileo Technology's (*www.galileot.com*) new core-logic chip for MIPS processors adds wider and faster memory and I/O buses to the features of its predecessors. The GT-64120 sports a 75-MHz interface to a MIPS processor, a 75-MHz interface to synchronous DRAM, and a 66-MHz PCI interface—all 64 bits wide. The PCI bus is particularly interesting because it can be split into two 32-bit interfaces. This latter arrangement is particularly useful for intelligent I/O (I_2O) applications with an upstream and a downstream PCI bus.

The GT-64120 is compatible with 64-bit SysAD buses, such as those on IDT's R4650, R4700, and R5000 and QED's RM5260, RM5270, and upcoming RM7000. In dual-PCI mode, the two expansion buses can run at different speeds and can even be set for different voltages (3.3 V or 5 V). In this arrangement, the chip could be used for a very high end I_2O controller for disks or networks; in single-PCI mode, it simply allows easy connection of SDRAM and peripherals.

The part, which comes in a large, 388-contact BGA, is priced at $60 in 10,000-unit quantities. Sampling now, the GT-64120 is slated to enter production in 1Q98. —*J.T.*