PA-8200 Grabs Performance Lead

Refusing to relinquish the performance crown to Digital, HP reasserted its position by rolling out workstations and servers based on a 236-MHz PA-8200. The new processor is rated at 16.3 SPECint95 (base) and 23.0 SPECfp95 (base), tying Digital's 21164-600 for the integer lead and extending HP's lead on the floating-point side (see MPR 10/6/97, p. 27).

When HP announced the PA-8200 (see MPR 10/28/96, p. 18), the company claimed the chip would reach 220 MHz and surpass the performance of all other microprocessors. The initial shipments (see MPR 6/2/97, p. 5) failed to satisfy either claim, reaching only 200 MHz and falling behind the performance of the Digital chip. Within a few months, however, HP identified and corrected the critical speed paths, boosting the clock speed beyond the initial plan and achieving performance leadership.

The first system to use the 236-MHz part is the Model C240 workstation, which lists for $46,000 with 1G of main memory, a 9G hard disk, a 20-inch color monitor, and no 3D acceleration. The 3D-graphics version of the system lists for $60,500 in the same configuration. Systems using the 200-MHz PA-8200 list for as little as $21,000.

This announcement shows the PA-8200 has reached its full potential and gives HP bragging rights over Digital, particularly on FP applications. HP could hold this position until next spring, when Digital's oft-delayed 21264 is expected to debut in systems. —*L.G.*

AMD Samples 0.25-Micron K6

Racing to keep pace with Intel, AMD has begun sampling chips from its 0.25-micron manufacturing process, a level that Intel reached just last month with its Tillamook processor (see MPR 9/15/97, p. 4). The first product in AMD's new process is a shrink version of its K6 processor, which is now sampling at a clock speed of 266 MHz.

When the K6 was launched (see MPR 3/31/97, p. 1), AMD expected to get some 266-MHz parts from its 0.30-micron process in 3Q97, followed by 300-MHz parts from the 0.25-micron process in 4Q97. While the IC process development is on track, the clock speeds are not. AMD has been unable to get adequate yields at 266 MHz from the older process, so these parts will not ship until 4Q97; the company now expects 300-MHz parts to ship early next year.

Because AMD's 0.30-micron process doesn't compare well with Intel's 0.28-micron process, Pentium II is currently shipping at 300 MHz, two speed grades faster than the K6. AMD's 0.25-micron process is much more competitive, however (see MPR 9/16/96, p. 11), which should move the K6 to within one speed grade of Pentium II. AMD says it will ship 350-MHz K6 processors in 2Q98 and 400-MHz parts by 4Q98; we expect 0.25-micron versions of Pentium II to be at 400 MHz in 2Q98 and 450 MHz by year's end.

AMD's new process also provides big savings in manufacturing cost and power dissipation. The die size of the new K6 is just 68 mm^2, less than half the size of the current version. This shrink cuts the K6's manufacturing cost from $70 to $40, according to the MDR Cost Model. It also raises the yield from roughly 75 to 275 good die per wafer, greatly increasing AMD's manufacturing capacity. Using the larger die, AMD has so far been unable to meet recent demand for the K6 (see MPR 9/15/97, p. 5), but the smaller part should solve this problem.

AMD did not release power numbers for the new part, but since the new process operates at 2.2 V instead of 3.3 V, the maximum power of the 266-MHz part should be well within the thermal envelope of Intel's Mobile Pentium parts, which go as high as 10 W. The current K6 is a bit too hot for notebooks; the new part will allow AMD to enter the smaller but more profitable mobile market, if the company desires. —*L.G.*

IBM Planning Shrink per Quarter for 6x86MX

The Cyrix-designed 6x86MX shipped a few months behind AMD's K6 and has not yet moved to a 0.25-micron process. The current chips, rated up to PR233 with a 187.5-MHz clock rate, are built in IBM's 0.35-micron CMOS-5X process. Even with the 6x86MX's per-clock performance advantage over the K6, it appears that AMD is going to pull ahead in the performance race with its 0.25-micron parts, putting pressure on IBM to rapidly move the 6x86MX into more advanced process technology.

IBM plans a 10% linear shrink to its CMOS-5X9 process by 1Q98, yielding a PR266 version using a 208-MHz CPU core and an 83-MHz bus speed. Just one quarter later, it plans to move to a 0.25-micron technology, CMOS-6S2, to deliver a PR300 version with an 83-MHz bus speed and a 250-MHz core frequency. And just one quarter after that, the company plans yet another shrink, this time to CMOS-6X, a more aggressive 0.25-micron process that will cut the power supply to about 1.8 V. This process is expected to enable a 100-MHz bus speed with a 250-MHz core, yielding a PR350 chip in 3Q98.

This roadmap appears to leave the 6x86MX one speed grade behind the K6's plans and two speed grades behind Intel's fastest parts. It should, however, enable the 6x86MX to serve the entry-level and midrange markets—at least where floating-point and MMX performance aren't critical. Cyrix will disclose at this month's Microprocessor Forum new devices that extend this roadmap. —*M.S.*

Tears of a Clone, Part II

With Steve Jobs now officially Interim CEO, Apple's position on Macintosh clones has been clarified in the past few weeks. Although Apple clearly doesn't want to compete with other Mac vendors, it has given Umax (which sells mainly outside

of Apple's home market) a reprieve, allowing that company to sell Macintosh systems, including the new Mac OS 8, until July 1998. In addition, Power Computing will be able to sell Macs with the new operating system through December of this year, when Apple's purchase of Power's Mac business (see MPR 9/15/97, p. 5) will be completed.

Despite these minor concessions, it appears the Mac clone era will end when the Umax agreement expires. Apple's other two Mac licensees, PowerPC partners Motorola and IBM, have both agreed to give up their licenses. IBM never participated in the Mac market, but Motorola had been moderately successful, selling more than 100,000 Mac systems; the company will take a $95 million writeoff to exit this business. In addition, both Motorola and IBM had sublicensed Mac OS to several companies, mostly in Taiwan, which will be forced out of the Mac market before they have even entered it.

Apple's refusal to support the "open" CHRP platform and continue licensing Mac OS reportedly violates the terms of the three companies' original partnership agreement (see MPR 7/24/91, p. 1), although none of the parties will confirm this. The companies have been engaged in a series of high-level discussions recently, attempting to redefine the partnership given the Macintosh's declining market share and potential changes in Apple's market strategies. These discussions could result in a reduction in the investment in future PowerPC processors for Apple, or even in radical changes in the Somerset PowerPC design center (see MPR 10/6/97, p. 3).

Adding to Apple's woes, erstwhile PowerPC chip vendor Exponential has filed a lawsuit against Apple, claiming the system maker broke an agreement to purchase Exponential's x704 chip, thereby driving the startup out of business (see MPR 6/2/97, p. 4). Apple's buyout of Power Computing and its concessions to Umax are seen as a way of avoiding lawsuits from those vendors over the termination of the clone market; if the negotiations with Motorola and IBM fall apart, those companies might end up suing Apple as well. With the Mac clone market about to draw its last breath, the legal vultures are circling in the sky. —*L.G.*

NEC Pushes R10000 to 250 MHz

Providing a stepping stone to next year's R12000 (see MPR 10/6/97, p. 1), NEC has begun volume shipments of a 0.25-micron version of the R10000 that achieves clock speeds of 250 MHz. As one might expect, this change increases performance on the SPEC benchmarks by about 25% over that of the 200-MHz R10000, to an estimated 13 SPECint95 (base) and 22 SPECfp95 (base). Most applications access main memory more than the SPEC programs do, however, and will thus see less of a boost from the faster part.

Should these SPEC estimates be achieved in systems, the new part would rank just behind the new 236-MHz PA-8200 (see MPR 10/6/97, p. 4) on SPECfp95, although it would trail both the HP part and Digital's 21164-600 by 20% on the integer side. Comparing these processors on price is rather difficult; the new R10000, like the HP and Digital products, has no published list price.

NEC originally expected to have its 0.25-micron process available in 1Q97, but difficulties in getting the process on line delayed shipment of the faster R10000. With the new process, the chip could probably operate as fast as 270 MHz, but this would require slowing the bus from 100 MHz to 90 MHz, reducing overall performance. Thus, NEC does not expect to offer any other speed grades of the 0.25-micron part, instead waiting for the R12000 to achieve speeds of 300 MHz with a 100-MHz bus.

The 0.25-micron process reduces the die size of the chip by about a third, from 298 mm^2 to 197 mm^2. Power dissipation falls nearly in half, from 30 W to 16 W (maximum), due mainly to a decrease in supply voltage from 3.3 V to 2.5 V. NEC believes these figures will position the part for high-end embedded applications, but the power dissipation is still too high for a network router or set-top box. Given the high prices NEC isn't quoting, the only customers are likely to be Silicon Graphics, Tandem, and Siemens-Nixdorf. —*L.G.*

Intel Ships Multilevel Flash Technology

Intel has announced its first flash-memory chip that encodes multiple bits in a single memory cell. The new technology, which Intel calls StrataFlash, uses each memory cell to hold four different voltages instead of the standard two. The four voltages can represent all possible states of two bits, allowing the cell to store two bits of digital information, twice as many as a standard memory cell.

This multilevel encoding technique solves a basic problem with flash: the size of the memory cell, which is a single transistor, is limited by the IC fabrication process (see MPR 5/30/94, p. 19). In a 0.4-micron process, which Intel uses to build its current parts, a single cell holds a charge of about 50,000 electrons. Intel's new sense circuitry, however, can detect variations in voltage corresponding to only 10,000 electrons. Theoretically, these sense circuits could be connected to tiny cells holding only 10,000 electrons, but the 0.4-micron process can't build cells that small.

Instead, the improved sense circuits can resolve multiple voltages from the same cell, effectively packing twice as many logical cells into the same physical space. Intel says the cell size of its Strataflash parts is the same as for its standard parts; the new circuitry to read and write multiple voltage levels adds about 5% to the total die area. The Strataflash parts are otherwise identical to the standard parts in specifications such as speed, error rate, and write cycles.

Despite this density advantage, Intel has announced only 32-Mbit and 64-Mbit chips so far, matching the maximum capacity of standard flash chips from vendors such as Samsung and Toshiba. Intel's 64-Mbit version carries a list price of $29.90 in quantities of 10,000. Other vendors have been working on multilevel flash technology, but Intel's is the first for digital devices to reach the market, which should give the company a price-per-bit advantage. —*L.G.*