by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send e-mail to belgard@umunhum.stanford.edu *with comments or questions.*

5,625,787

Superscalar instruction pipeline using alignment logic responsive to boundary-identification logic for aligning and appending variable-length instructions to instructions stored in cache
Issued: April 29, 1997
Inventors: Stephen W. Mahin, et al
Assignee: IBM
Filed: May 12, 1995
Claims: 20
A superscalar microprocessor with variable-length instructions includes logic that handles self-modifying code.

5,623,628

Computer system and method for maintaining memory consistency in a pipelined, nonblocking caching-bus-request queue
Issued: April 22, 1997
Inventors: James M. Brayton, et al
Assignee: Intel
Filed: March 2, 1994
Claims: 13
A computer system and method with a cache-consistency mechanism. The consistency mechanism includes an external bus-request queue for reads and writes.

5,623,627

Computer-memory architecture including a replacement cache
Issued: April 22, 1997
Inventor: David B. Witt
Assignee: AMD
Filed: December 9, 1993
Claims: 21
A microprocessor with an on-chip first-level cache and an on-chip victim cache. The victim cache is at least half the size of the first-level cache and is clocked only when accessed.

5,623,619

Linearly addressable microprocessor cache
Issued: April 22, 1997
Inventor: David B. Witt
Assignee: AMD
Filed: July 24, 1995
Claims: 45
An x86 processor with a cache that is linear-address addressable. Included are physical-to-linear, linear-to-physical, logical-to-linear, and linear-to-logical address translators.

5,623,617

Method for decoding sequences of guest instructions for a host computer
Issued: April 22, 1997
Inventor: Gary G. Davidian
Assignee: Apple
Filed: June 7, 1995
Claims: 18
Common instruction sequences or repeated sequences in a guest program are detected during emulation of the guest program on a host processor, and performance of the emulation is optimized based on the detected sequences.

5,623,615

Circuit and method for reducing prefetch cycles on microprocessors
Issued: April 22, 1997
Inventors: Gaby J. Salem, et al
Assignee: IBM
Filed: August 4, 1994
Claims: 19
A microprocessor and method that inhibit prefetching of instructions from an instruction cache when the required instructions are already present within a prefetch buffer.

5,623,614

Branch-prediction cache with multiple entries for returns having multiple callers
Issued: April 22, 1997
Inventors: Korbin S. Van Dyke, et al
Assignee: AMD
Filed: September 17, 1993
Claims: 25
A branch-prediction cache selects from among multiple branch-address entries for a single return instruction that returns to multiple callers. When a program address has multiple matches in the branch-address associative memory, the return-address associative memory enables only the entry that has an associated return address matching the top of the RtnStack.

5,619,668

Apparatus for register bypassing in a microprocessor
Issued: April 8, 1997
Inventor: Syed A. A. Zaidi
Assignee: Intel
Filed: September 22, 1994
Claims: 16
A microprocessor has at least two ALUs. Attached to the output of each ALU is an output latch. Either of the latches may supply input to either of the ALUs to effect register bypassing. M