Motorola Updates ColdFire Core to V3

As Motorola's midrange 32-bitter approaches adolescence, it is undergoing some internal changes. Motorola has released details of ColdFire V3, a microarchitectural alteration that will allow future ColdFire chips to keep up with industry-wide advances in clock speed and performance. The first ColdFire 3 chips are expected to debut in 1H98.

To allow for faster clock rates, V3 extends ColdFire's pipeline by two stages. Instruction decoding and operand reads now take two cycles apiece. The instruction buffer has also been enlarged to hold eight instructions rather than 12 bytes (3–6 instructions). The longer pipeline means branch instructions actually take longer than before (in terms of clock cycles), but this penalty will be offset by V3's faster peak clock rate, which Motorola expects to reach 100 MHz.

To alleviate some of the branch penalty, ColdFire V3 implements a new form of branch "hinting." Programmers can use a new global control bit to reverse ColdFire's usual prediction for forward branches (i.e., taken vs. not taken). For software that knows which way branches are likely to go, this new feature can eliminate many mispredictions.

All the changes to the pipeline allow Motorola to support higher frequencies and clock multiplication for the first time with ColdFire. Whereas today's parts are limited to about 33 MHz, next-generation ColdFire parts will reach 90–100 MHz in the next 18 months, according to the company. Fabrication will also move to 0.35-micron technology from the quaint 0.8-micron methods used now.

Motorola expects that most ColdFire V3 parts will include a hardware multiply-accumulate (MAC) unit, which few ColdFire chips have now, and that they will support an integer divide instruction for the first time.

The company predicts that 90-MHz ColdFire V3 parts will be nearly 3× faster than current 33-MHz V2 parts—which is hardly surprising, given the nearly 3× difference in clock speed. The longer pipeline, clock doubling, and branch hinting merely allow ColdFire to keep up with its clock rate. Clock-for-clock, ColdFire performance will be unchanged.

Overall, Motorola's alterations to ColdFire are nothing spectacular; they merely keep ColdFire on the growth path the company outlined last year (see MPR 9/16/96, p. 1). The company will make similar updates every year or two to keep ColdFire on an upward performance track. For Motorola, ColdFire is neither its fastest nor its cheapest product line, but it does hold the broad middle ground and forms the basis of a number of ASIC and ASSP designs. As long as ColdFire keeps growing up, it will always have a parent—and customers—that continue to love it. —*J.T.*

68K-to-ColdFire Software Translator Emerges

At long last, Motorola has produced a translator that converts assembly source code from 68000 to ColdFire. Although the two families share a similar hardware architecture and instruction set, they are not binary compatible, and users have been forced to manually rewrite assembly code when moving from one Motorola processor to the other.

The translator, called PortASM/68K/CF, was not developed by Motorola but was licensed from a British company, MicroAPL. In addition to the basic 680x0 processors, the translator can translate code from the CPU32 and CPU32+ cores used in several 68300-series integrated processors. The translator runs under Windows 3.x, 95, NT, Solaris, and SunOS but not, ironically, on Macintosh or other Motorola-based systems. PortASM/68K/CF translates only assembly source code; binary translation remains a fond dream.

Recognizing the need for such a tool three years after the fact, Motorola distributes the translator for free; support, however, costs $500 per year. Users can download the program from *www.motorola.com/isd*. —*J.T.*

IDT R4700 Hits 200 MHz

IDT has boosted the top speed of its FPU-equipped R4700 microprocessor to 200 MHz. The 64-bit chip is now as fast as IDT's high-end part, the R5000, and is nearly as expensive. At $130 in large quantities, the R4700 is among the more expensive embedded processors available, although it is also one of the few with top-end floating-point capability.

Embedded 64-bit processors are few, and ones with FPUs are fewer, but QED and NEC have entered this market with lower-priced parts. The RM5270 (see MPR 10/27/97, p. 11) has an FPU as well as an L2 cache-control unit and sells for just $100 at 200 MHz . NEC's R4310 MIPS processor (see MPR 10/27/97, p. 11), at 167 MHz, isn't quite as fast as the R4700, but it does have an FPU—and at just $25, it's one-fifth the price of IDT's chip.

The market for FPU-equipped chips is growing quickly as high-end page printers sell in record numbers. Floating-point arithmetic is important for PostScript, and the high bandwidth of a 64-bit bus is helpful as well. IDT's target market is on a strong upward slope, but potential customers may find its prices a bit steep. —*J.T.*

New Core-Logic Support for M32R/D

Mitsubishi's unusual CPU-in-a-DRAM combination chip, the M32R/D (see MPR 5/27/96, p. 10), now has two companions. The company recently announced the M65439 and M65544, two core-logic support chips for the novel microprocessor, both of which are available immediately.

Both chips include a DRAM controller (which is not as superfluous as it sounds) for external memory, a DMA controller, interrupt logic, 16-bit timers, and at least two UARTs. The two chips differ in the PC Card and LCD interface: the '439 includes a two-slot PC Card controller, while the '544 comes with a passive-color LCD controller. The latter part

also has more timers and serial channels.

Both parts come in a 176-lead TQFP package (although they are not pin-compatible) and are currently in volume production. In 10,000-unit quantities, the ’439 is priced at $10; the ’455 costs $12. —*J.T.*

Digital Swings Across Two New PCI Bridges

Digital Semiconductor (R.I.P.) added two new PCI bridge chips to its already swollen portfolio of such devices. The 21553 and 21554 are the company’s first “embedded” PCI bridge chips, fulfilling a particular role within that product category. The two chips are nearly identical; the ’553 has a 32-bit PCI interface, while the ’554 has a 64-bit bus.

More interesting is what makes these two chips different from normal PCI bridges: instead of a transparent passage between upstream and downstream PCI buses, the ’553 and ’554 keep the buses separate. In an I_2O system, the host processor is unaware of devices on the downstream bus and does not map them into its address space during device enumeration. For such systems, the ’553 and ’554 include an I_2O messaging unit for communication with the host processor.

In effect, the ’553 and ’554 allow designers to create a StrongArm-based I_2O controller similar to Intel’s i960RP or ’RD devices (see MPR 6/19/95, p. 10) but without the Intel processor. Or, given recent events (see MPR 11/17/97, p. 1), perhaps with just a different kind of Intel processor. —*J.T.*

Toshiba Spins 74-MHz Windows CE Processor

Toshiba has released one of the first commercial products to come out of its R3900 “Southern Cross” development (see MPR 2/16/95, p. 20), the R3912, a low-power processor for handheld devices. The new chip runs at 74 MHz and dissipates an average of 300 mW, placing it among the more power-efficient 32-bit processors available.

Like virtually all low-power MIPS chips these days, the R3912 includes a hardware MAC unit for soft-modem emulation. The part also includes the TLB required by Windows CE, a 4K instruction cache, a 1K data cache, an IrDA port, and a PCMCIA controller. Toshiba rates the 3.3-V part at 78 Dhrystone MIPS.

The R3912 is a dead ringer for NEC’s R4102 (see MPR 4/21/97, p. 4). Both have the same instruction set, cache sizes, Windows CE support, target markets, and $25 price in 10,000-unit quantities. The Toshiba device is a bit faster, while the NEC chip includes A/D functions. Power dissipation is comparable, given their differences in clock speed. NEC has already scored (its own) handheld PC design win; the Toshiba chip lurks in some Japanese consumer items. Both chips show that MIPS, and Windows CE, are making deeper inroads into the growing consumer market. —*J.T.*