Intel Plans Low-Cost Pentium II Products

Intel has confirmed plans to offer two new versions of its Pentium II processor in 1998, both aimed at low-cost PCs. The first is a version of the module without L2 cache; this part is set to appear in mid-1998. The second product incorporates the L2 cache onto the processor chip. Because this part requires changing the CPU itself, it probably won't appear until late 1998.

With much of the growth in the PC market coming at the low end (see MPR 11/17/97, p. 3), Intel wants to make sure Pentium II can participate at these price points. Even with the forthcoming 0.25-micron Deschutes, we estimate the cost of the module to be $70, much more than the $45 Pentium/MMX chip. Thus, selling the Deschutes module for the same $100 price as a low-end Pentium/MMX would reduce Intel's margins—something the company doesn't want to do.

Eliminating the 512K cache and possibly trimming other packaging costs could shave $5–$10 from Pentium II's manufacturing cost, a significant margin improvement. These changes could be made while still allowing the cacheless module to plug into the same Slot 1 interface. Of course, a Pentium II with no L2 cache would have poorer performance, but probably no worse than a Pentium/MMX of the same clock speed on most applications. This performance would be adequate for low-end systems.

Integrating the L2 cache would solve the performance problem. Because the on-chip cache would presumably operate at the full CPU speed and could be set associative, it could be smaller than the current external cache—perhaps 128K or 256K—while providing similar performance. In a 0.25-micron process, a 256K cache would add about 30 mm^2 to the die, but the cost of the package could be reduced by eliminating the external cache interface.

Overall, adding the L2 cache on chip could increase the manufacturing cost of the processor by about $5–$10. But by getting rid of the external cache, this module would cost less than the current module with similar performance. The on-chip cache would also be ideal for notebooks, since it saves space and reduces power consumption. Thus, this design could become widely used in notebooks and mainstream desktops in 1H99.

The objectives of this strategy are clear: eliminate Socket 7 from Intel's product line as quickly as possible without giving up on the low-cost PC market. Because Pentium II uses Intel's proprietary Slot 1 technology, other x86 vendors plan to stick with the more open Socket 7 throughout 1998. By moving completely to Slot 1 by mid-1998, Intel can pull the rug out from under its competitors, forcing PC makers to maintain a different motherboard solely for the non-Intel parts. While Socket 7 will certainly remain viable after Intel ceases to use it, this move will make it more difficult for Intel's competitors to gain PC design wins. —*L.G.*

Cyrix Readies MediaGX With MMX

Cyrix is preparing an enhanced version of its low-end MediaGX processor (see MPR 3/10/97, p. 1) that adds MMX capability. The new chip, code-named GXm (GX multimedia), retains the 5x86 integer core but adds the fast FPU and MMX unit from the 6x86MX. The new chip also upgrades the EDO DRAM controller to support 100-MHz SDRAM.

Cyrix expects the initial clock frequencies to be 200 and 233 MHz. The GXm will be built in the same 0.35-micron four-layer-metal technology as the current MediaGX chips, which are now shipping at speeds of up to 200 MHz. The jump to 233 MHz comes from circuit rework.

The GXm enables the MediaGX family to keep up with the advances in Intel's low-end offerings; it won't move the family upscale, but it should keep it from falling further behind. Without the addition of MMX, the MediaGX would have had a hard time holding any market position in 1998. The big boost will come with the MXi, due in 2H98, which is based on the Cayenne CPU core (see MPR 10/27/97, p. 22) and includes an advanced 3D graphics accelerator. —*M.S.*

S3 Brings 3D to Business Desktops

Combining its successful Virge 3D engine with a new 128-bit GUI accelerator, S3's new Trio3D provides the features business users need—excellent 2D performance and low cost—along with checkbox 3D acceleration and basic support for digital video. Trio3D is sampling now. When S3 ships this new chip in the first half of 1998, it will be priced at $22 in 10,000-unit quantities.

With this announcement, S3 (*www.s3.com*) debuts a new 336-pin BGA package it plans to use for future consumer and business 3D products. The larger package supports 125-MHz SGRAM and provides extra pins for expansion; we expect to see full AGP support and possibly a 128-bit local-memory interface on 1998 products. S3 has recently acquired a license to use Rambus memory technology, and we also expect to see Direct RDRAM support in future S3 chips. For use in existing Trio64 and Virge products, the company will also offer Trio3D in a pin-compatible 208-pin PQFP. —*P.N.G.*

Bug Makes Some Pentium Systems Vulnerable

Intel has acknowledged a bug in all Pentium/MMX and Pentium processors that could enable malicious users to crash unprotected Internet servers. If a "lock" prefix is applied to a CMPXCH8B mem64 instruction that invalidly uses a 32-bit register (instead of a 64-bit memory value) as a destination operand, the processor comes to a complete halt. The correct response would be to signal an invalid operand exception. Since this instruction encoding is invalid, there is no reason for any compiler to produce the instruction or for any application to use it.

Thus, PC users running standard applications should never encounter this problem. The significance of the bug comes from the fact that a user with a shell account at an Internet service provider with the privilege to execute machine code directly could run a script that triggers the bug. There would be no reason for doing so other than malice, but it makes any system that gives users the ability to run user code subject to being deliberately crashed. (Note that clever and malicious users can find many other ways to create havoc in such systems.)

Intel believes there are potential workarounds, and it hopes to release further details by mid-November. These workarounds would probably be in the operating system and would only need to be applied on servers and other systems providing remote access; most PC users would not need to be concerned. Intel has no plans to recall processors or offer replacement parts due to this bug. —*M.S.*

IBM Speeds P2SC, Deploys First 64-Bit Chip

Two new systems from IBM improve the performance of the RS/6000 family *(www.rs6000.ibm.com)* in two different ways. The Model 397 uses a 160-MHz version of the P2SC processor (see MPR 8/26/96, p. 14) that offers 20% better performance than the previous P2SC. The company also rolled out its first 64-bit RS/6000 system, the Model S70.

The Model 397 is rated at 7.1 SPECint95 (base) and a stellar 22.4 SPECfp95 (base). Although the integer score is no better than Pentium/MMX's, the floating-point score trails only HP's 236-MHz PA-8200 and Digital's 21164-600 among currently shipping systems.

The new processor is identical to the original P2SC except for a shrink to IBM's CMOS-6S2 process (see MPR 9/16/96, p. 11), a 0.25-micron hybrid process with metal layers similar to those of a 0.35-micron process. The new process improves the clock speed by about 20% while reducing the die size from 355 mm^2 to 256 mm^2. Due to its enormous die and 1,088-pin package, the older P2SC had the highest manufacturing cost of any current microprocessor, according to the MDR Cost Model; the new version reduces the estimated cost from $375 to $290, better but still more than any shipping CPU.

The Model 397 includes the 160-MHz P2SC, 128M of memory, and a 4.5G hard drive (but no monitor or graphics acceleration) for a list price of $29,900. IBM will also offer the faster PS2C in its SP line of parallel supercomputers.

For nearly two years, IBM has been shipping 64-bit AS/400 systems based on two "PowerPC AS" processors known as the A10 and A30 (see MPR 7/31/95, p. 15); these chips implemented the PowerPC instruction set along with special extensions to support older AS/400 software. The PowerPC 620 was supposed to be the first true PowerPC chip with 64-bit capabilities, but that processor floundered, and IBM now says it will not ship any 620-based products.

Instead, the company is selling a system based on a new processor called the RS64. This chip was derived from the A10 but eliminates the AS/400-specific instructions. The chip acts as a stopgap solution until the 64-bit Power3 (seeMPR 11/17/97, p. 23) arrives next year.

The new S70 system uses a 125-MHz RS64 processor with 64K of instruction cache and 64K of data cache on chip. The standard configuration includes four CPUs, each with 4M of external cache, plus 512M of memory and 4.5G of hard disk, all at a list price of $125,000. It comes with AIX 4.3, a new version of IBM's Unix operating system that includes full 64-bit support.

IBM's RS/6000 is the last of the major RISC product lines to gain a 64-bit processor. Digital and Silicon Graphics have been shipping 64-bit systems for years and offer this capability in all of their current systems; Sun and HP came later to the party but now have 64-bit processors in all but their low-end systems. Although the number of applications that take advantage of 64-bit support remains small, 64-bit addressing provides a significant performance boost when working with large data bases and large scientific data sets. Adding this capability will allow IBM to better compete in these high-end applications. —*L.G.*

TI Adds Floating Point to 'C62xx

Revving up its floating-point engine, Texas Instruments disclosed plans for the 320C67xx DSP, which adds floating-point capability to its EPIC-like 320C62xx DSP (see MPR 2/17/97, p. 14). The 'C67xx uses the same basic instruction set as the fixed-point 'C62xx, which will allow programmers to more easily move their code from one family to the other. Surprisingly, TI is the first DSP vendor to offer a common instruction set for both fixed- and floating-point DSP chips.

The 'C67xx core will be capable of six 32-bit floating-point operations per cycle, resulting in a peak execution rate of 1 GFLOPS at 167 MHz. This clock speed is slightly slower than that of the 'C62xx when built in the same 0.25-micron (drawn) five-layer-metal process. Still, this level of floating-point performance is well ahead of what is available in today's DSP chips, as TI has let its floating-point DSPs stagnate over the past few years.

The device is still a ways away: production parts won't ship until early 1999. TI says it will provide a follow-on part by the end of the decade that delivers 3 GFLOPS. The company did not announce specific products or pricing but said the 'C67xx parts will be priced about the same as current 'C3x and 'C4x chips, including some priced below $50.

Many DSP designers prototype algorithms in floating-point arithmetic but use fixed-point chips for volume production, due to their lower cost. The 'C67xx will make it easier for designers to make this move. In addition, its high performance will improve the capabilities of advanced signal-processing applications such as voice recognition, cellular-telephone base stations, radar, and finite-element analysis. The combination of the 'C62xx and 'C67xx should give Texas Instruments the undisputed performance lead for both fixed- and floating-point DSP applications. —*L.G.* M