by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send comments or questions via e-mail to belgard@umunhum.stanford.edu.

5,628,024

Computer architecture capable of concurrent issuance and execution of general-purpose multiple instructions
Issued: May 6, 1997
Inventor: Robert W. Horst
Assignee: Tandem
Filed: June 7, 1995
Claims: 6
A system for issuing a family of instructions during a single clock. Logic attached to the instruction decoder determines whether resource conflicts would occur if the family were issued during one clock. If no resource conflicts occur, an execution unit executes the family regardless of whether dependencies among the instructions in the family exist.

5,628,021

System and method for assigning tags to control instruction processing in a superscalar processor
Issued: May 6, 1997
Inventors: Kevin R. Iadonato, et al
Assignee: Seiko Epson
Filed: April 4, 1994
Claims: 62
In an out-of-order microprocessor, a register file stores data for each instruction. A queue contains instructions and tags. The tags are arranged in the queue in program order. Data for instructions can be read out of the register file in program order based on the tags.

5,627,983

Processor architecture providing out-of-order execution
Issued: May 6, 1997
Inventors: Valeri Popescu, et al
Assignee: Hyundai
Filed: June 6, 1995
Claims: 18
An out-of-order processor that includes a shelving unit for temporarily storing instructions to issue and to temporarily receive results of execution; functional units to perform the instructions; and a retirement unit to commit instructions.

5,627,985

Speculative and committed resource files in an out-of-order processor
Issued: May 6, 1997
Inventors: Michael A. Fetterman, et al
Assignee: Intel
Filed: January 4, 1994
Claims: 33
An out-of-order processor that contains, and interconnects, a register alias table, a reorder buffer, and a reservation station.

5,627,993

Methods and systems for merging data during cache checking and write-back cycles for memory reads and writes
Issued: May 6, 1997
Inventors: Richard P. Abato, et al
Assignee: IBM
Filed: April 29, 1996
Claims: 8
In response to memory reads or writes from a secondary processor, data is transferred into a buffer during a snoop cycle to a cache. The data in the buffer is merged with write-back data from the cache in a write operation. Data is provided directly from the buffer to the secondary processor and to main memory in a read operation.

5,627,992

Organization of an integrated cache unit for flexible usage in supporting microprocessor operations
Issued: May 6, 1997
Inventor: Gigy Baror
Assignee: AMD
Filed: May 4, 1995
Claims: 32
A computer system having a cache that allows setting of caching policies on a page basis and a line basis. A status field for each cache block controls whether the cache-control unit operates in a write-through or copy-back write mode when a write hit access to the block occurs.

5,627,981

Software mechanism for accurately handling exceptions generated by instructions scheduled speculatively due to branch elimination
Issued: May 6, 1997
Inventors: Michael C. Adler, et al
Assignee: Digital
Filed: July 1, 1994
Claims: 12
A method for generating an exception when a speculative instruction is committed. An exception flag, associated with the speculatively executed instruction, is tested at the commit point of the instruction. If it indicates an exception, an exception is raised at the commit point. M