First VSI Project Exposes Challenges

Toshiba's 1904AF MIPS Chip Uncovers Bumps in System-on-a-Chip Road Map

by Jim Turley

The highly vaunted Virtual Sockets Initiative, which was developed to allow open "snap together" chip development, has claimed its first success. But the project was not without its problems, and some holes in the current VSI specification have been uncovered. Consequently, the industry still has far to go before the vision of modular, interchangeable blocks of chip-level logic exchanged between unrelated companies comes to pass.

Toshiba's TMP1904AF (see MPR 8/4/97, p. 9) is the first microprocessor to be developed entirely with VSI-compliant logic blocks and design processes. The low-end embedded CPU includes Toshiba's TX19 MIPS core, dual caches, a DRAM controller, and some basic peripherals. In all, the chip includes 14 distinct VSI logic blocks, according to Toshiba and Cadence, which collaborated on the design of the chip.

As two of the founding members of the VSI Association (*www.vsia.org*) Cadence and Toshiba were logical partners for this collaborative effort. Although Cadence had participated in third-party designs that used one or more VSI "components" (chip-level macro functions described according to VSI specifications), the 1904AF was the first chip to include nothing but VSI components.

Spec Defines How, Not What Component Does

As it stands, VSI specification 1.0 defines a level of documentation for each component. Prospective VSI component suppliers must define the function's operation, timing, and physical details using a standard format. For testing, claims and assumptions must be specified, including verification methods (usually test vectors) for those claims and assumptions. Finally, a design database (i.e., Verilog description) of the part itself must be included so the part can be integrated into the whole.

Each VSI component must implement a standalone function. That is, it must be able to work without relying on the presence or function of any companion blocks. For example, if a memory controller requires a timer, the timer must be included in the definition of the controller.

Both parties rapidly realized the need to fill in numerous details of the VSI specification for real chip designs. The initial specification was too general and lacked the kind of specific definitions and requirements that would allow trouble-free integration of unfamiliar components. For example, there is no physical or logical specification for the interface between components. Each logic block can be designed with its own data requirements and signaling conventions.

Toshiba and Cadence found that this level of detail does nothing to guarantee that components work together (or that they work at all). Rather, the design team had to design each component (serial port, SRAM array, timer, etc.) as a self-contained, standalone function and then knit it together with the others. The matter was simplified by the fact that all 14 components came from within Toshiba; intercompany transfer of VSI components is not yet feasible.

The project thus avoided the issue of security or theft. Currently, VSI does not include provisions for protecting components from unauthorized use or intellectual-property theft. Because the component must be described completely, including an RTL description of its function, any component can be reverse-engineered. For high-value functions such as microprocessor cores, security can be a major issue.

For the time being, these issues must be dealt with using legal or contractual means. For example, a component is often licensed for "one-time" use, or for limited use on a specified number of projects. Alternatively, component licenses are sometimes sold together with design services; the component is useless without the services of the component provider. Advanced RISC Machines, for example, generally dispenses its embedded cores in this manner.

Work Under Way to Fill the Holes

There are several groups at work within VSIA to solve these problems. For security, design files could be "watermarked" to discourage unauthorized use; encryption is another possibility. A standard for an internal, chip-level bus interface is also under consideration.

To help eliminate glue logic among components, or between components and an on-chip bus, future VSI components may be required to use the proposed standard intermediate bus interface, similar to a software API (application programming interface). Chip designers could then rationalize their efforts, designing a single "translator" block between the standard VSI interface and the actual on-chip bus in their design. Beyond that, a VSI protocol-level specification is also in the works. In conjunction with the physical-level spec, it would allow components to communicate with each other.

Despite the hurdles, engineers at both Cadence and Toshiba remain enthusiastic about VSI. The designers of the 1904AF believe that even though VSI components are not easily interoperable or interchangeable across corporate boundaries, the level of documentation that VSI enforces makes these components more usable than a random macro function might otherwise be. Given more time, they believe, integrating components from multiple sources may eventually become simpler and more common. M