by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send e-mail to belgard@umunhum.stanford.edu *with comments or questions.*

5,634,135

Microprocessor with priority determination and priority-based instruction selection
Issued: May 27, 1997
Inventor: James F. Hollander
Assignee: TI
Filed: December 13, 1991
Claims: 28
An out-of-order microprocessor that executes certain instructions in an order determined by a priority memory or program within the microprocessor. Instructions that may be issued out of order are given priority by the memory or the priority program and are then issued in the determined order.

5,634,131

Method and apparatus for independently stopping and restarting functional units
Issued: May 27, 1997
Inventors: Eugene P. Matter, et al
Assignee: Intel
Filed: October 26, 1994
Claims: 32
Disclosed is an integrated circuit with multiple function units using individual clocks. At least one function unit has circuitry that detects that the function unit is not in use and disables the clock to that unit. Also shown is circuitry that determines imminent use of the powered-down function unit and re-enables the function unit's clock.

5,634,103

Method and system for minimizing branch misprediction penalties within a processor
Issued: May 27, 1997
Inventors: Carl D. Dietz, et al
Assignee: IBM
Filed: November 9, 1995
Claims: 18
A method and system for decreasing branch misprediction penalties within a superscalar processor with branch prediction. If a conditional branch occurs in the instruction stream and is predicted taken, instruction fetch is started at the taken address. However, if the processor has already fetched the sequential (i.e., not taken) instruction, and there are function units available for dispatch, then the sequential instruction is speculatively dispatched.

5,632,037

Microprocessor having power-management circuitry with coprocessor support
Issued: May 20, 1997
Inventors: Robert Maher, et al
Assignee: Cyrix
Filed: March 27, 1992
Claims: 8
A microprocessor with a coprocessor, or a system that contains a microprocessor with a coprocessor, has power-management circuitry. The power-management circuitry responds to both the coprocessor busy signal and an external signal. The power-management circuitry disables the clock to the core when the external signal is asserted and busy is not asserted.

5,632,023

Superscalar microprocessor including flag operand renaming and forwarding apparatus
Issued: May 20, 1997
Inventors: Scott A. White, et al
Assignee: AMD
Filed: June 1, 1994
Claims: 50
An out-of-order superscalar microprocessor whose reorder buffer contains a flags storage area for storing flag results. The flags are renamed to make possible earlier execution of the branch instructions that depend on flag-modifying instructions.

5,630,157

Computer organization for multiple and out-of-order execution of condition-code testing and setting instructions
Issued: May 13, 1997
Inventor: Harry Dwyer, III
Assignee: IBM
Filed: October 25, 1994
Claims: 6
A system with an out-of-order superscalar processor that binds instructions that set condition codes to immediately succeeding instructions that use those codes so the instructions are executed as a single unit.

OTHER ISSUED PATENTS

5,634,118 *Splitting a floating-point stack-exchange instruction for merging into surrounding instructions by operand translation*
5,634,047 *Method for executing branch instructions by processing loop end conditions in a second processor*
5,634,025 *Method and system for efficiently fetching variable-width instructions in a data-processing system having multiple prefetch units* M