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NEC VR5400 Makes Media Debut

NEC/Sandcraft Project Produces High-End Embedded Processor

by Jim Turley

For embedded designers who want it all, a wish may soon be granted. Later this year, NEC will begin producing the VR5464, a new embedded part festooned with high-end features: superscalar execution to six execution units, double-precision floating point, enormous dual 32K caches, a 100-MHz bus interface, multimedia extensions, and a SIMD vector unit, as Figure 1 shows. If it weren't priced at only $70, NEC's VR5464 would make a respectable desktop processor.

Instead, the VR5464 and VR5432 (which differ only in external bus width) are aimed at office-automation products due to appear around the end of this year. They will complement NEC's VR43xx midrange MIPS chips and its VR41xx portable-processor series. Competition will come from similar MIPS devices from QED as well as the newly released embedded PowerPC EC603e from IBM and Motorola.

Sandcraft Teams With NEC for Now

The debut of the VR54xx is something of a coming-out party for Sandcraft, the Santa Clara (Calif.) startup that codesigned the chips with NEC. The 30-person company was formed in 1996 from ex-HP and MIPS Technologies personnel including president Norm Yeung, engineering VP Mike Gupta, and chief engineer Ed Pak, all of whom worked on the VR4300. The firm has toiled in obscurity for the past 18 months, devoted to its sole client and its first full-scale design.

The R54xx core design is jointly owned by Sandcraft and NEC, although NEC is guaranteed a period of exclusivity in return for its investment in the project. The company poured several million dollars into the project, but the funding was purely to cover development expenses; NEC has no equity stake or ownership in Sandcraft.

Following the release of the VR5464 and '32, Sandcraft and NEC will assume an arm's-length relationship; the first will court new clients, and the second will begin work on its own derivatives of VR54xx parts. NEC says several application-specific variations of the VR5432 and '64 are planned, but it isn't ready to announce a schedule.

Sandcraft (*www.sandcraft.com*) is focusing on MIPS-based designs, preferring to capitalize on its experience with the VR54xx core rather than strike out in a new direction. Because Sandcraft does not have a MIPS license, its clients will have to be licensees themselves, namely IDT, LSI Logic, NEC, NKK, Philips, QED, Siemens, Sony, and Toshiba.

Sandcraft has no plans to become a fabless chip company in the QED mold. Instead, it holds up ARM as a business model to be emulated: an intellectual-property company supplying core CPU designs to licensed fabricators. Company marketing VP Dirk Smits compares Sandcraft's relationship to its clients "as Pratt & Whitney is to Boeing," supplying "propulsion" for another's products.

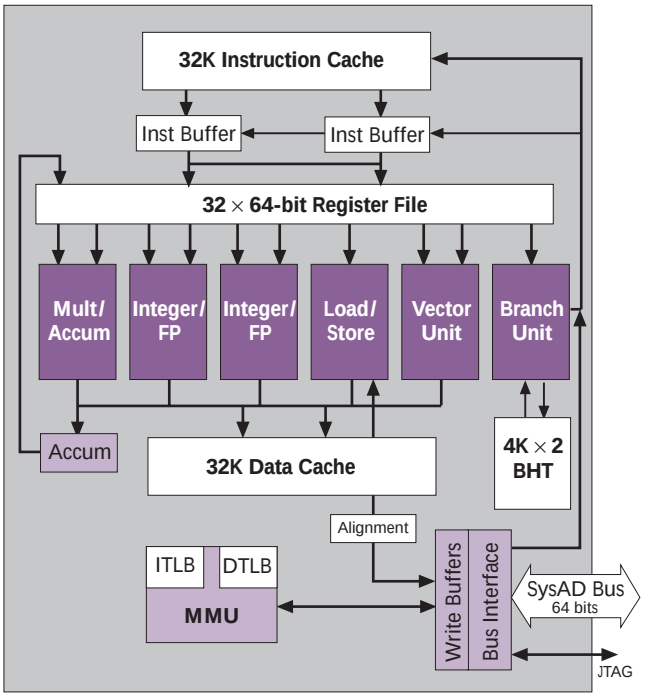

Figure 1. NEC's VR5400 chips dispatch two instructions to a set of six execution units, including two identical integer/FP units.

In-House R5400 Core Breaks With MIPS Tradition

NEC has flaunted its independence in recent years, designing the VR4100, VR4200, and now the VR54xx parts by itself rather than using Silicon Graphics cores as feed stock. The VR5400 core owes little to Silicon Graphics other than its underlying MIPS-IV instruction set and MDMX influences.

Even those instruction sets underwent some significant tweaking. The VR54xx parts add 16 forms of multiply-accumulate instructions, a user-level instruction to prefetch data into the data cache, a new conditional move that is not part of the standard MIPS-IV definition, indexed loads and stores, and, in a heretical break from MIPS doctrine, a rotate instruction. The MDMX instructions, in contrast, have been trimmed back.

The chip issues instructions to a collection of six execution units. All six units can be busy at once, although only two instructions may be issued in any one cycle. The two integer/FP units are identical, so most programs can dispatch their instructions in pairs. Instructions can complete out of order but are committed to the register file in order, two at a time. The CPU also includes branch prediction (with a 4,096-entry BHT), write buffers, micro-TLBs, and nonblocking access to the data cache.

Performance Approaches Workstation Level

NEC believes its VR5464 will crank out 10.0 SPECint95 and 4.5 SPECfp95 (peak) at 250 MHz, similar to the performance of a low-end Pentium II. Both the VR5464 and '32 are aimed not at workstations but at high-end laser printers, network routers, and other line-powered equipment with a voracious appetite for bandwidth and a need for floating-point arithmetic, media acceleration, or both.

NEC also claims a whopping 519 Dhrystone MIPS for the same part, a ratio of better than 2.0 MIPS/MHz. Both the SPEC and the Dhrystone numbers are purely estimates, however. The smaller, integer-only Dhrystone benchmark was compiled and then run on an RTL simulation of the VR5464, where memory speed and bandwidth don't matter. The SPEC numbers are just extrapolations based on the performance of an R5000, with allowances made for the different clock speed, dispatch rate, bus protocol, bandwidth, cache organization, and myriad other differences between these two chips. Nonetheless, NEC defends its SPEC estimates as being a little on the conservative side.

Mnemonic	Description
ADD.xx, SUB.xx, MUL.xx	Saturating arithmetic
AND, OR, NOR, XOR, SLL, SRL	Logicals and shifts
MAX, MIN, PICK.xx	Select
WACx, RACx, RZU	Access accumulator
C.xx	Compare
ALNI, SHFL	Byte alignment
DROR, DROR32, DROV, ROR, RORV	Rotate 32, 64 bits
MACC, MACCHI, MACCHIU, MACCU	Multiply-add
MSAC, MSACHI, MSACHIU, MSACU	Multiply-subtract
MUL, MULHI, MULHIU, MULU	Multiply, no accumulate
MULS, MULSHI, MULSHIU, MULSU	Multiply, subtract from 0

Table 1. NEC's VR54xx chips include more than 30 new instructions, including several media-processing operations.

The VR5464 taped out in early February, just two months behind NEC's original schedule. The first samples are due to arrive from the Tokyo fab in April, and NEC says it expects the chip to be in production by September. This schedule seems awfully optimistic in light of the usual 12-month lag from tape-out to production we've witnessed for chips of this complexity. A more traditional schedule would put production in 1Q99. The 32-bit VR5432 is slated to follow its wide-bus sibling by about 2–3 months.

Media Enhancements Similar to Mad Max

The VR54xx chips are the first MIPS processors to support any kind of multimedia extensions. Silicon Graphics described MDMX (MIPS digital media extensions, affectionately called Mad Max) more than a year ago (see MPR 11/18/96, p. 24) but provided no timetable for its debut. The VR54xx implements features very similar to MDMX but is not technically (or legally) compatible with SGI's specification. NEC shies away from using the term MDMX in its literature and prefers to call the enhancements simply "multimedia extensions."

The VR5432 and '64 have several new instructions for arithmetic and logical operations on packed bytes, as Table 1 shows. The 31 new media instructions operate on eight unsigned bytes packed into a single register in coprocessor CP1. Many operations accumulate, and others saturate. Per MDMX guidelines, the VR54xx has a 192-bit accumulator, segmented into eight 24-bit accumulators, to prevent overflows caused by repeated media-processing operations.

Although the VR54xx's media extensions were created to satisfy a specific customer's needs, all of the instructions are equivalent to ones already defined by MDMX. So, to prevent software incompatibilities, each new VR54xx instruction is encoded the same way as its analogous MDMX instruction. Legally, NEC is not an MDMX licensee, but in practical terms, the VR54xx is software-compatible with MDMX nonetheless.

The VR54xx implements only a subset—about one-quarter—of the complete MDMX extensions. Most 8-bit MDMX operations are duplicated on the VR54xx, but none of the 16-bit or 32-bit operations are supported at all. Any unsupported MDMX instruction causes an unimplemented-instruction fault, as it would on any other MIPS processor.

NEC defends its decision to sidestep full MDMX compatibility by citing customer demand. Customers making laser printers want to accelerate image compression and decompression, NEC says, and don't need anything more than 8-bit precision. The added cost of a full MDMX implementation wasn't worth the extra silicon area or the added design and verification time.

Hardware Is Compatible With R5000

The hardware interface to the VR5432 and '64 is similar to the R5000's. In fact, NEC claims that the '64 is pin-compatible with the R5000, despite the fact that the latter has an extra L2 cache bus that the two embedded chips don't.

The L2 cache pins are present but (mostly) unconnected on the VR54xx parts. The R5000's connection to an initialization PROM is now used to select the VR54xx's clock multiplier; a debug interface also occupies some L2 bus pins. Power and ground are found in the same place as on the R5000, although V_{CC} is now split between a 2.5-V core supply and a 3.3-V pad ring. Theoretically, a carefully designed circuit board could accept either an R5000 or a VR5464, both of which use a 272-contact BGA package.

NEC Goes Head-to-Head With QED

As Table 2 shows, the VR54xx chips stack up well against a number of other high-end embedded processors, combining the best features of many with a price that's somewhere in the middle. Like the plethora of products clustered around the $25 price point, there is now a second embedded price/performance tier forming in the $65–$75 range.

The VR5432 and '64 compare most closely with a pair of sister chips from QED, the RM5230 and RM5260. Like NEC's new parts, the QED devices are MIPS-IV based, with high clock rates, large caches, full FPUs, and a choice of 32-bit or 64-bit external buses.

It's tough at first to spot the differences. Compared with QED's RM5260, the R5464 runs at the same or faster clock speed (200 or 250 MHz), uses about the same amount of power (4 W), issues the same number of instructions per clock (two), has a double-precision FPU, has a similar hardware MAC, has similar cache locking and preloading, and has the same internal and external bus width (64 bits).

Although both parts are loosely based on the R5000 and can nominally dispatch two instructions per clock, NEC's VR54xx is considerably more flexible than QED's chips. The VR54xx CPU can execute any combination of integer and floating-point instructions at once (or an integer/FP paired with a vector, load/store, or branch), whereas the RM52xx CPU can start two instructions only if one is an integer operation and the other is for the FPU. For code that is FP-rich, or—which is more likely—filled with integer code, the VR54xx can give twice the effective throughput. Also in NEC's favor: the VR54xx has a unique vector unit, twice the cache, and is built in a more advanced IC process. On the downside, the VR54xx needs a split power supply instead of the RM52xx's single 3.3-V source.

Depending on an OEM's production schedule, these differences may not matter. The VR54xx chips don't enter production until late this year (versus immediate availability of the QED parts), so they're more appropriate for systems in the 1999 time period and beyond. Customers with a shorter fuse may prefer to use the RM52xx parts right away.

NEC's price is a bit higher than QED's. The VR5464 is 15% more expensive at 200 MHz ($70 vs. $60); the 250-MHz version is a lot more expensive, at $95. In sum, NEC charges an extra $10 for the vector unit and the bigger caches. Com-

	VR5464	VR5432	RM5270	RM5260	RM5230	i960HT	Pentium	603e	EC603e	SA-110	SH7750
Architecture	MIPS	MIPS	MIPS	MIPS	MIPS	i960	x86	PowerPC	PowerPC	ARM	SuperH
Vendor	NEC	NEC	QED	QED	QED	Intel	Intel	IBM/Mot	Motorola	Digital	Hitachi
Frequency	250 MHz	167 MHz	200 MHz	200 MHz	175 MHz	80 MHz	233 MHz	200 MHz	266 MHz	233 MHz	200 MHz
Execution units	6	6	2	2	2	2	2	5	4	1	2
Issue/clock	2	2	2	2	2	2	2	3	2	1	2
FPU?	yes	yes	yes	yes	yes	no	yes	yes	no	no	yes
Hardware MAC?	yes	yes	yes	yes	yes	no	no	yes	yes	yes	yes
Vector operations?	yes	yes	no	no	no	no	yes	no	no	no	yes
Caches (I/D)	32K/32K	32K/32K	16K/16K	16K/16K	16K/16K	16K/8K	16K/16K	16K/16K	16K/16K	16K/16K	8K/16K
L2 cache interface?	no	no	yes	no	no	no	no	no	no	no	no
Cache locking?	yes	yes	yes	yes	yes	yes	no	no	no	no	no
Bus width	64 bits	32 bits	64 bits	64 bits	32 bits	32 bits	64 bits	64 bits	64 bits	32 bits	64 bits
Cache snoop?	no	no	no	no	no	no	no	yes	yes	no	no
Memory controller?	no	no	no	no	no	no	no	no	no	no	yes
Fab process	0.25µ	0.25µ	0.35µ	0.35µ	0.35µ	0.35µ	0.25µ	0.35µ	0.35µ	0.35µ	0.25µ
Voltage (V)	2.5/3.3	2.5/3.3	3.3	3.3	3.3	3.3	2.8	2.5/3.3	2.5/3.3	1.65/3.3	1.8/3.3
Power (typical)	4.4 W	2.5 W	4.0 W	4.0 W	3.6 W	4.5 W	12.0 W	4.0 W	4.8 W*	1.1 W	1.5 W
Dhrystone MIPS	519	347	260	260	227	125	168	282	376	268	360
SPECint95	10 (est)	n/a	5.5	5.0	4.0	n/a	7.1	5.6	6.7	n/a	n/a
SPECfp95	4.5 (est)	n/a	6.1	5.2	4.2	n/a	4.2	4.9	n/a	n/a	n/a
Price (10K)	$95	$45	$75	$60	$35	$69	$193†	$58	$81	$49	$40
Availability	3Q98	4Q98	now	now	now	now	now	now	now	now	3Q98

Table 2. A comparison of high-end embedded processors shows that NEC's new VR5400 parts combine the best features of many of its competitors but won't enter production until one year later. (Source: vendors, except *MDR estimates) †1,000-unit quantity.

Price & Availability

NEC's VR5464 will begin sampling in April. The VR5432 will begin sampling in August. Production quantities of the VR5464 and '32 are scheduled for September and November, respectively. In 10,000-unit quantities, the 167-MHz VR5432 will be priced at $45; the VR5464 is priced at $70 for 200 MHz and $95 for 250 MHz.

For more information, contact NEC Electronics (Santa Clara, Calif.) at 800.366.9782 or direct your browser to *www.nec.com/products/products.html*.

parisons between the narrow-bus VR5432 and RM5230 are similar, with the price difference still just $10. Realistically, these small price differences probably won't matter in real negotiations.

VR54xx Holds FPU Over PowerPC

The top-end VR5464 is more expensive (by $14) than the Motorola/IBM EC603e, is slower by a mere 11 MHz, but has valuable floating-point and vector units that the embedded PowerPC lacks. In return, the EC603e retains its multimaster bus with snooping, obvious remnants of the EC603e's history as a desktop processor. This makes the VR54xx a clear winner over the PowerPC chip for PostScript printers or motion-control systems that need floating-point capability; in networking, where bandwidth is vital, the two are about even. If anything, the PowerPC has the advantage of socket compatibility with even faster PowerPC devices like the 740 and 604 chips.

If the VR5464 were available today, it would make an even more attractive purchase than the already compelling EC603e. But again, by the time the NEC chips are shipping, competitors' prices will have fallen, and newer embedded PowerPC chips may be available. Given the rapid decline of PowerPC prices, new chips probably aren't far off.

Floating-Point Now Common, Vector Unit Less So

Floating-point units are becoming more common in this price range, which is dominated by erstwhile desktop processors. In floating-point performance, the VR54xx chips are strong but not record-breaking. As it did with the VR4300, NEC designed the integer and FP pipes as a single execution unit to save space. FP latency is usually 2–6 cycles, with the notable exceptions of FP divide, square root, and reciprocals, which take anywhere from 30 to 120 cycles to complete. The VR54xx chips hold their own against competitive RISC processors and nose ahead of the congested, stack-based FPU in Pentium.

The PowerPC 603e and 604e have outstanding floating-point performance but are still priced as desktop processors, not embedded chips. The EC603e has its FPU disabled, giving Motorola and IBM a rationale for lowering its price significantly. Hitachi's SH7750 sports a double-precision FPU and a vector unit of sorts, and it is priced well below NEC's asking price. Unlike the VR54xx, however, the SH7750 can't execute two integer (or two FP) instructions simultaneously, and its vector unit is designed specifically for 3D setup rather than media processing.

Vector Capability Orthogonal to MMX and SH-4

For vector capability, embedded designers have few choices: Pentium/MMX, Hitachi's new SH7750, and the VR54xx twins. Pentium's MMX is roughly comparable in scope to NEC's new vector operations. Both perform SIMD (single instruction, multiple data) logical and arithmetic operations on 8-bit quantities to accelerate certain media subroutines. Both are limited to simple integers (a design decision Intel will correct in Katmai). The VR5432 and '64 also support vector-to-vector operations and a 24-bit accumulator, which Pentium can't match. Conversely, MMX offers a much broader and richer set of instructions, many of which work on 16-bit quantities, making MMX useful for video and audio work.

Hitachi's vector unit is quite different from those in the VR54xx or Pentium. It is intended to accelerate polygon setup in concert with, ironically enough, NEC's PowerVR 3D graphics chips. Apart from its two geometry instructions, the SH-4 is not inherently equipped for the kind of media processing that MMX or the VR54xx extensions allow.

VR5400 Should Aid Profit Picture

NEC's two new parts will be potent competitors when they enter the market later this year. At just $45 to $95 in volume, they're also priced attractively. Were it not for QED's recent steep price reductions on its RM52xx chips, the VR5464 and '32 would have been nearly alone in high-end embedded price/performance.

As inexpensive as they are, these two chips should be profitable for NEC. Weighing in at 5.8 million transistors and 47 mm^2 (of which 40% is cache) in NEC's 0.25-micron three-layer-metal process, the VR54xx parts cost just $25 to build, according to the MDR Cost Model. At these prices, NEC can afford to be a little aggressive in its pricing, putting pressure on QED and others that rely on third-party foundries. Even IBM and Motorola will feel the pressure from these new MIPS competitors.

NEC has already lined up OEM customers for its part—it never would have undertaken the design without them—so it has some reason to believe it can recoup its investment with Sandcraft. NEC won't disclose its customers, but likely users are current R5000 customers looking for a 1.5× performance boost in integer code and an even bigger gain in media-manipulation performance. Cisco, Hewlett-Packard, Ricoh, EFI, and Bay Networks are just a few obvious candidates. If the VR54xx parts get the same reception the VR4300, NEC has a good 1999 ahead of itself. M