AUDIO/VIDEO

3D graphics accelerator chips. An overview of 3D technology and products that are currently available. Charles Ostman, *Midnight Engineering*, 2/98, p. 49, 10 pp.

BUSES

Intelligent I/O: Does I_2O hold H_2O? By offloading interrupt and bus-traffic overhead caused by standard I/O operations, intelligent I/O subsystems allow host CPUs to support more users or transactions. Now, the I_2O initiative seeks to make such subsystems both OS- and hardware-independent, leading to widespread deployment. Maury Wright, *EDN*, 3/2/98, p. 56, 8 pp.

CPU

Alpha vs. Pentium II. The two most powerful chips in the Windows NT domain face off. Tom Yager, *Windows NT Systems*, 4/98, p. 55, 6 pp.

Optical processing paradigms for electronic computers. Used as special-purpose architectures, optical or optoelectronic processing systems can enhance the performance of electronic computers. Pericles A. Mitkas, Colorado State University, et al; *Computer*, 2/98, p. 45, 7 pp.

Microprocessor and DSP technologies unite for embedded applications. Many embedded applications require a mixture of CPU and DSP functions; semiconductor vendors are creating hybrid devices to handle both types of processing. Markus Levy, *EDN*, 3/2/98, p. 73. 7 pp.

DEVELOPMENT TOOLS

Analog and digital oscilloscopes. Here is a sampling of recently introduced analog and digital scopes in all price ranges. *Electronic Products*, 2/98, p. 31, 4 pp.

DSP

Superscalar processor delivers 400 MIPS for DSP and control needs. The ZSP 16401 scalable DSP engine quickly executes complex algorithms thanks to dual MACs, dual ALUs, and a 200-MHz clock. Dave Bursky, *Electronic Design*, 2/9/98, p. 37, 4 pp.

DSP IC's clock oscillator uses inexpensive crystals. Circuit trick eliminates a DSP chip's need for expensive, low-ESR crystals. Sergey Dickey, Dynamic Telecommunications; *EDN*, 3/2/98, p. 127, 3 pp.

IC DESIGN

Add testability now to core-based chips or pay later. Knowing the available design-for-test techniques and EDA tools to implement these techniques helps you over your system-on-a-chip test hurdles. Jim Lipman, *EDN*, 2/16/98, p. 65, 7 pp.

MEMORY

Analyzing and implementing SDRAM and SGRAM controllers. Designing your own synchronous-DRAM controller lets you tune its cost, complexity, and performance to your application needs. You've got lots of options, so research the trade-offs before proceeding. Christian Greene, MoSys; *EDN*, 2/2/98, p. 155, 7 pp.

MISCELLANEOUS

The big squeeze. Forget 300-mm wafers. Over the next few years, techniques that shrink die size will be the most important technology trend. Lawrence J. Curran, *Electronic Business*, 3/98, p. 51, 4 pp.

PROGRAMMABLE LOGIC

Streamlined RAM-based family of FPGAs trims system cost. Packing 5,000 to 40,000 gates, the high-density Spartan family of FPGAs from Xilinx competes with mask-programmed gate-array costs. Dave Bursky, *Electronic Design*, 2/23/98, p. 98, 2 pp.

Variable-grain architecture pumps up FPGA performance. Highly efficient logic and interconnect allow Vantis's VF1 family to deliver 250-MHz operation. Dave Bursky, *Electronic Design*, 2/23/98, p. 102, 3 pp.

SYSTEM DESIGN

Software debugging on a single-chip system. More and more of the system is being packed into fewer and fewer chips. But when you finally get down to a one-chip system, how do you debug the software? Eric Ryherd, *Embedded Systems Programming*, 3/98, p. 66, 6 pp.

Don't be afraid of debugging symmetric multiprocessing systems. These tips can help you tame your system problems, using conventional logic-analysis tools and the Pentium Pro architecture. Michael Patterson and John Freidman, Hewlett-Packard; *Electronic Design*, 2/23/98, p. 42, 5 pp.

Bus interface logic evolves to meet VLSI needs. The VCX family of VLSI circuit interfaces is driving down delays and power in bus-support logic. Dave Bursky, *Electronic Design*, 2/23/98, p. 91, 4 pp.

Design conference becomes launch pad for portable components. The latest products and technologies boasting small size and reduced power are unveiled at Portable By Design. Richard Nass, *Electronic Design*, p. 59, 2 pp.

Reap benefits while simplifying dual-battery portable power management. Power-path-controller ICs can effectively switch power among various power sources in a minimum of board space; at the same time, they meet smart-battery standards. Mark Gurries and Timothy Skovmand, Linear Technology; *EDN*, 2/16/98, p. 117, 6 pp.

Termination techniques for high-speed buses. Choosing the proper bus-termination technique—parallel, series, Thevenin, AC, or diode-based—is critical to digital-system performance. Karthik Ethirajan and John Nemec, California Micro Devices; *EDN*, 2/16/98, p. 135, 9 pp.

Programmable logic overcomes processor bottlenecks. When the application requires additional computing power, programmable logic can do more than just decode access to memory and peripherals. Steve Knapp, *Personal Engineering*, 3/98, p. 48, 4 pp.