by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send e-mail to belgard@umunhum.stanford.edu *with comments or questions.*

5,659,782

System and method for handling load and/or store operations in a superscalar microprocessor
Issued: August 19, 1997
Inventors: Cheryl D. Senter, et al
Assignee: Seiko Epson
Filed: September 16, 1994
Claims: 38
In an out-of-order superscalar microprocessor, a method and hardware for managing load and store operations. Load requests are made out of order whenever the load is known to have no address collisions and no writes pending.

5,659,703

Microprocessor system with hierarchical stack and method of operation
Issued: August 19, 1997
Inventors: Charles H. Moore, et al
Assignee: Patriot Scientific
Filed: June 7, 1995
Claims: 8
A microprocessor with a push-down stack. The top section of the stack is implemented in registers and is backed by a second section in RAM, both on-chip. Those sections are further backed by another section in system RAM.

5,657,483

Computer system with power-management feature for stopping the internal clock of a microprocessor
Issued: August 12, 1997
Inventors: James P. Kardach, et al
Assignee: Intel
Filed: September 27, 1995
Claims: 4
A computer system, particularly a laptop, that includes a microprogrammed microprocessor. The microcode stops execution of instructions in the microprocessor when the computer system is idle.

5,655,133

Massively multiplexed superscalar Harvard architecture computer
Issued: August 5, 1997
Inventors: Wayne P. Dupree, et al
Assignee: Dow Chemical
Filed: November 13, 1995
Claims: 21
A VLIW CPU with multiple independent dedicated execution units. Each has a separate result bus multiplexed to all general-purpose registers. The general-purpose registers have output ports to connect to at least one of the execution units. A separate data-control circuit is further provided to achieve a Harvard architecture design for the CPU.

5,655,132

Register file with multitasking support
Issued: August 5, 1997
Inventor: George A. Watson
Assignee: Rockwell
Filed: August 8, 1994
Claims: 7
A register file and a method for managing it to permit rapid task and context switching. Each register has an absolute address. A relative register address is used in instructions. A per-task base address is indexed to obtain an absolute register address. Different sets of registers may be thereby designated for different tasks or contexts.

5,655,115

Processor structure and method for watchpoint of plural simultaneous unresolved branch evaluation
Issued: August 5, 1998
Inventors: Gene W. Shen, et al
Assignee: Hal Computer Systems
Filed: June 7, 1995
Claims: 73
Time-out checkpoints are formed on the basis of a predetermined number of instructions issued or the number of clock cycles elapsed, for example. Time-out checkpointing limits the maximum number of instructions within a checkpoint boundary and bounds the time period for recovery from an exception condition.

5,655,098

High-performance superscalar microprocessor including a circuit for byte-aligning CISC instructions stored in a variable byte-length format
Issued: August 5, 1997
Inventors: David B. Witt, et al
Assignee: AMD
Filed: February 9, 1996
Claims: 37
A CISC superscalar microprocessor that speculatively executes RISC instructions (ROPs) translated from the CISC instructions. Multiple instructions may be retired in a single cycle. Retirement of speculative instructions is prevented on instructions past incorrectly predicted conditional branches and allowed on correctly predicted branches.

PATENT WATCH

5,655,097

High-performance superscalar microprocessor including an instruction-cache circuit for byte-aligning CISC instructions stored in a variable byte-length format
Issued: August 5, 1997
Inventors: David B. Witt, et al
Assignee: AMD
Filed: February 9, 1996
Claims: 20
A CISC superscalar microprocessor (e.g., the K6) that translates CISC instructions into RISC ROPs. The instruction cache stores the CISC instructions and predecode bits; it prefetches, predecodes, and aligns the instructions. The instruction decoder receives these aligned instructions and translates them into sequences of ROPs.

5,655,096

Method and apparatus for dynamic scheduling of instructions to ensure sequentially coherent data in a processor employing out-of-order execution
Issued: August 5, 1997
Inventor: Michael H. Branigin
Filed: August 25, 1993
Claims: 2
A method for operating an out-of-order processor with out-of-order retirement. Instructions are executed when there are no remaining data dependencies or antidependencies. Coherency handling for exception conditions in such a processor is given.

5,652,894

Method and apparatus for providing power-saving modes to a pipelined processor
Issued: July 29, 1997
Inventors: King Seng Hu, et al
Assignee: Intel
Filed: September 29, 1995
Claims: 6
A clock-and-reset unit provides power-saving modes to a pipelined microprocessor. A register in the clock-and-reset unit is used to provide a power-saving mode. When the register is written to select power saving, the processor is stalled and the clocks are frozen.

5,652,872

Translator having segment bounds encoding for storage in a TLB
Issued: July 29, 1997
Inventors: David E. Richter, et al
Assignee: Exponential Technology (now S3)
Filed: May 8, 1995
Claims: 20
A processor emulates x86 segment-bounds checking with a paging system. References to addresses within pages fully contained within a segment are not checked against a segment limit. References to addresses within pages not fully contained within a segment are limit-checked against the offset within the page.

5,651,125

High-performance superscalar microprocessor including a common reorder buffer and common register file for both integer and floating-point operations
Issued: July 22, 1997
Inventors: David B. Witt, et al
Assignee: AMD
Filed: July 10, 1997
Claims: 28
A superscalar microprocessor with an integer unit and a floating-point unit that share a main data bus. The integer unit and the floating-point unit also share a common reorder buffer, register file, branch-prediction unit and load/store unit, which all reside on the main data bus.

5,649,174

Microprocessor with instruction-cycle versus clock-frequency mode selection
Issued: July 15, 1997
Inventor: Kenneth A. Dockser
Assignee: VLSI
Filed: December 9, 1994
Claims: 10
A processor and methods that selectively allow the processor to operate at two clock frequencies. When the processor operates at the higher clock frequency, an instruction that is comprised of multiple operations occurs in multiple cycles. When the processor operates at the lower clock frequency, the operations execute in a single clock cycle.

OTHER ISSUED PATENTS

5,655,141 *Method and system for storing information in a processing system*
5,652,774 *Method and apparatus for decreasing the cycle times of a data-processing system*
5,651,124 *Processor structure and method for aggressively scheduling long-latency instructions, including load/store instructions while maintaining precise state*
5,649,178 *Apparatus and method for storing and initializing branch prediction with selective information transfer*
5,659,721 *Processor structure and method for checkpointing instructions to maintain precise state* M