IDT RC32364 Tops in Price/Performance

New Midrange MIPS Part First in Series of Enhanced MIPS-I Designs

by Jim Turley

Integrated Device Technology (IDT) has produced the first 32-bit microprocessor to top 10 MIPS/dollar. The new RC32364 processor offers terrific performance for its price, drastically undercutting the best PowerPC and StrongArm processors. IDT is revamping its midrange CPU line, starting with a redesigned R3000 processor core. The new core is an IDT-only derivative that first appears in the company's new '364 chip, sampling now.

The new part replaces IDT's existing—and rapidly aging—line of R3000 processors like the R3081 by offering far better performance and more features at a lower price. The R30xx family will continue serving the lowest price levels while the newer 32364 is appealing for new designs. IDT's performance claims are, however, based on simulation and not actual measured performance.

MIPS-IV Features in MIPS-I Clothing

After acquiring the R4640 and R4650 from QED (see MPR 11/14/94, p. 18), IDT built a design team to work on the 36100 (see MPR 10/27/97, p. 11). The new 32300 core design is the second effort from that team and reinvigorates the company's line of general-purpose CPUs.

The 32300 core is conceptually similar to Toshiba's TX39 (see MPR 2/16/95, p. 20). In both cases, the developer took the basic MIPS-I (R3000) 32-bit processor core and added features from successive generations but stopped short of a complete 64-bit R5000-style core.

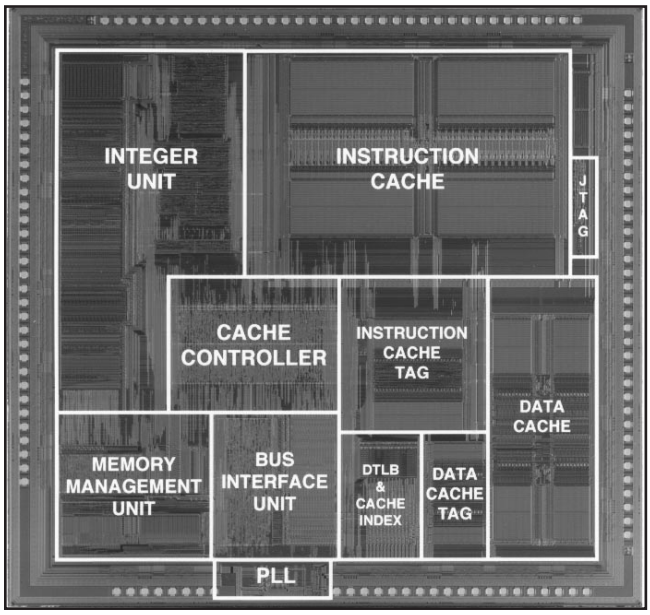

Figure 1. Die photo of the 29-mm^2 R32364 shows the large amount of area devoted to the 8K instruction cache and that the PLL encroaches on the pad ring.

The new instruction-set extensions include conditional moves, cache prefetching, branch-likely instructions, and nonblocking loads. IDT also added a multiply-accumulate instruction, which is not part of any official MIPS instruction set but is *de rigueur* for any new CPU these days.

In short, IDT's 32300 core has all the features of an R5000-series core except the 64-bit registers and ALU. IDT has found that the new features are more valuable to customers than the 64-bit data paths. They're more economical, too. IDT was able to update its existing R3000-series core without licensing and paying the higher royalty rate for a MIPS-IV design.

With the exception of some high-end printers and routers, few applications need a full 64-bit MIPS-IV processor in an embedded application, but some MIPS-IV features are clearly useful. Unfortunately, MIPS Technologies has not defined such a core, leaving IDT to create its own. As with the multiply-accumulate function, lack of guidance and control from MIPS has forced the licensees to strike out on their own, defining individual—and sometimes mutually incompatible—implementations.

Nonblocking Loads Remove Bottlenecks

The nonblocking loads are not an instruction-set addition but an internal microarchitectural enhancement. By adding a second write port to the register file, the 32300 core is able to continue processing while a load operation is outstanding. The chip is smart enough to interlock on load-use conflicts while the load is still pending. Cache misses load the critical word first, allowing processing to continue while the remainder of the line is loaded.

Nonblocking caches have appeared in desktop processor for years. They improve performance in a general sense and are valuable to embedded designers because they allow for checking I/O registers (which are typically slow to respond) without stalling the processor. They also enable another of the 32300's interesting features: cache prefetching.

Using the PREF instruction, programmers can ask the processor to preload the data cache from a specified address. The chip will comply if it's convenient; that is, as long as the extra bus cycles don't interfere with normal code fetches or data handling. At run time, the programmer has no way to know whether the data was actually prefetched or not. If so, there should be some performance improvement. If not, there's no harm done. The MADD (multiply-add) instruction is compatible with MADD from IDT's R4650, which makes it

incompatible with similar instructions on LSI Logic chips. Multiply-accumulate is one of the areas where the MIPS licensees have blazed their own trails rather than following a unified path set out by MIPS Technologies.

First Chip Has Little I/O

The first use of IDT's 32300 CPU is the RC32364, a standard part that is already sampling and is due to enter production in 3Q98. The '364 marries the core with a pair of caches, an MMU, and a bus interface. The part is just a foretaste of a series of integrated controllers to come, according to IDT.

The feature set of the '364 holds no surprises. The 8K instruction cache and 2K data cache are both lockable on a line-by-line basis; the data cache can be configured for either write-back or write-through updates. The MMU (including a 16-entry data TLB) will support Windows CE. The chip's 32-bit external bus won't do dynamic bus sizing, but space for 8- and 16-bit devices can be efficiently mapped onto the bus with a simple reconfiguration of the bus-interface unit.

The chip is built using IDT's 0.35-micron three-layer-metal process. As the die photo in Figure 1 shows, the chip's 29 mm^2 of area is spent largely on cache, a technology IDT knows well. The CPU core occupies some 4 mm^2 of silicon, about the same size as an ARM7 or IBM's PowerPC 401 core. The chip is built using IDT's 0.35-micron three-layer-metal process.

Although it's not apparent from the die photo, IDT is using an internal hardware bus to join the core, caches, and bus interface. With the bus, IDT can quickly add peripherals to the basic design, much as Motorola does with its IMB (intermodule bus) on many 683xx devices. IDT correctly believes integrated components, not generic processors, will be the key to unlocking many high-volume applications. In particular, the company is interested in providing processors, not just memories, to networking companies. This is a market where its chips are already popular and where unit volume is growing quickly. If IDT can enlarge its presence with these customers, revenue should rapidly follow.

Performance Leads Rest of IDT's Line

With claimed performance of 175 MIPS (Dhrystone 2.1) at 133 MHz, the RC32364 delivers more than 1.3 MIPS/MHz. This ratio is high for a scalar MIPS design, which would generally yield about 1.1–1.2 MIPS/MHz. These numbers are simulated, even though IDT is shipping samples of the chip. The company doesn't believe actual scores will differ.

Though the final performance numbers may change, the 32364's modest price of $16.50 (in 10,000-piece lots for the 133-MHz chip) is not in doubt. If IDT's performance estimates hold true, the '364 will deliver better than 10 Dhrystone MIPS per dollar, the first 32-bit processor we've tracked to reach this milestone.

As Table 1 shows, QED's high-end RM5230 and NEC's VR4310 and VR5432—MIPS parts, every one—are the runners up with about 8–9 Dhrystones/dollar. IDT's own R3041 and R3081 chips (see MPR 11/18/92, p. 23) are well below this level, a sign of their advancing age. Even Intel's famous SA-110 falls well behind this mark, although it still excels in terms of power efficiency.

For straightforward, nonintegrated, unadorned microprocessors, the RC32364 has many competitors but no equal. It doesn't have the FPU of NEC's VR43xx chips, the pin-compatibility of the PowerPC EC603e, or the remarkable current conservation of StrongArm, but unless users have a particular antipathy toward MIPS chips, the '364 is the best bargain for around $15.

Integration on the Way

Although the chip has no on-chip peripherals to speak of, IDT has integration in mind. The '364 is just an appetizer; the main course comes in 4Q98 when the first application-specific versions start sampling.

Fully 60% of IDT's revenue comes directly from makers of networking and telecommunications equipment, mostly from SRAM and FIFO chips. With its foot firmly in the door, IDT can start to enlarge its sales to these customers. If it is successful, it will muscle out NEC, Motorola, and QED for the more lucrative microprocessor business.

With networking, data communications, and telecommunications markets growing swiftly, there are plenty of new design wins to pursue. And if the 32364 is any indication, the 32300 makes a most excellent pursuit vehicle. M

Price & Availability

IDT's RC32364 is sampling now; production is scheduled for 3Q98. In 10,000-unit quantities, the part will be priced at $12.50 for 100 MHz or $16.50 for 133 MHz.

For more information, contact IDT (Santa Clara) at 800.345.7015 or visit *www.idt.com/products/risc/welcome.html*.

	IDT R32364	IDT R32364	IDT R4640	QED RM5230	NEC VR4310	NEC VR5432	Motorola EC603e	Intel SA-110
Arch.	MIPS	MIPS	MIPS	MIPS	MIPS	MIPS	PowerPC	ARM
Frequency	133 MHz	100 MHz	200 MHz	100 MHz	166 MHz	347 MHz	100 MHz	233 MHz
MIPS*	175 MIPS	131 MIPS	265 MIPS	175 MIPS	210 MIPS	141 MIPS	141 MIPS	268 MIPS
MIPS/dollar	**10.6**	10.5	9.1	8.8	8.4	7.7	6.8	5.5
Cache (I/D)	8K/2K	8K/2K	8K/8K	16K/16K	16K/8K	16K/16K	16K/16K	16K/16K
Power (typ)	0.85 W	0.64 W	1.8 W	1.9 W	1.8 W	3.2 W	3.2 W	0.36 W
Price (10k)	$16.50	$12.50	$29	$20	$25	$45	$20.69	$49

Table 1. IDT's RC32364 is the first 32-bit processor to deliver better than 10 MIPS/dollar. *based on Dhrystone 2.1. (Source: vendors)