MoSys Returns to the Mainstream

Company Ships New "1T-SRAM" and Fast SGRAMs

by Peter N. Glaskowsky

MoSys is one of the few fabless semiconductor firms in the memory industry. Although the company has been quiet for the past few years, it has recently introduced new SGRAMs and cache SRAMs that should recapture the attention of major PC system and graphics-card vendors.

Early Products Weren't Compatible

With major investors including Integrated Device Technology (IDT), MoSys *(www.mosys.com)* got its start with MDRAM, a multibank DRAM aimed at the graphics market that was faster than any other graphics memory but also incompatible with every other graphics memory. MDRAM (see MPR 12/25/95, p. 17) achieved a couple of minor design wins, but major customers stayed away. The parts were too difficult to support and faster than the market needed at the time.

The company's next product was MCache, a DRAM-based device designed to replace SRAMs in Pentium L2 cache applications. MCache (see MPR 5/6/96, p. 16) was developed when SRAMs were particularly expensive. With each MCache chip being about a third the size of an SRAM of the same capacity, MoSys was able to offer highly competitive pricing on these parts. Early problems with MCache's unique handshaking protocol for refresh cycles, and the subsequent crash in SRAM prices, kept MoSys from selling as many of the parts as it had hoped, but it has still found buyers for some five million MCache parts.

MoSys has kept a low profile, but it hasn't given up its dream of achieving mainstream success with its unconventional memory-chip designs. While R&D continued, MoSys made a strategic decision to withhold public product announcements until OEMs were actually shipping systems with its new products.

DRAM Becomes Compatible SRAM

This milestone has finally been achieved, and MoSys is ready to talk. The company has announced two new MCache parts, now renamed "1T-SRAM," that are exact functional replacements for the pipelined-burst SRAMs currently used in Socket 7 systems. With DRAM arrays that operate at unprecedented speeds, the new chips can hide their precharge and refresh operations from the outside world. The chips look and act in every way like 100–133 MHz 512-Kbyte SRAMs that are organized as 64K × 64 or 128K × 32—except that power consumption is much lower in normal operation because they *are* still DRAMs. Small cores and effective row caches reduce wire loading and core accesses for typical access patterns. Even in worst-case modes (a row miss on every access), power consumption is no worse than commodity SRAMs of the same density. Standby power isn't as low as for micropower SRAMs, but MoSys is willing to cede that niche market.

As if to prove these new chips really are transparently identical to SRAMs, MoSys has developed flow-through and late-write versions. These parts are meant for use in the telecomm and datacomm markets.

The pipelined-burst chips are also compatible with the Pentium II's L2 cache chips for processors up to 333 MHz, and the next shrink should support 500-MHz processors. Unfortunately for MoSys, Intel is adequately served by its current SRAM suppliers and seems unlikely to use the new 1T-SRAMs.

MoSys is focusing on the Socket 7 market, where it now has design wins in Sony notebooks and various desktop clone motherboards. In addition to single-chip 512K caches, MoSys can provide 1M and 2M cache solutions for 100-MHz Socket 7 configurations. This could improve the performance of Socket 7 processors such as AMD's K6-2 for Windows NT, which is highly sensitive to L2 cache size.

MoSys Also Claims Fastest SGRAMs

While other SGRAM vendors are stretching to reach 125-MHz speeds in production and 150 MHz on paper, MoSys is shipping 200-MHz parts based on 0.35-micron process technology—and 250-MHz parts are due next year. Even the fastest announced graphics chips (see MPR 8/3/98, p. 1) run their local memory at only 200 MHz, so MoSys is clearly ahead of the demand curve.

Peak bus bandwidth isn't the whole story on the new SGRAMs. At speeds up to 166 MHz, these chips offer two-clock latencies, one cycle faster than parts from all other vendors. Graphics-chip accesses average 4–7 data phases per access, MoSys says, so the quicker SGRAMs produce an extra 80–200 Mbytes/s of sustained bandwidth compared with conventional SGRAMs at the same clock rate.

MoSys plans to support double-data-rate (DDR) transfers on SGRAMs at or above 166 MHz, feeling the payoff for DDR isn't worthwhile at slower clock speeds. The company says its 166-MHz single-data-rate two-clock-latency parts permit higher effective bandwidth than 125-MHz DDR three-clock-latency parts.

MoSys SGRAMs are being used on reference designs for graphics accelerators from 3Dlabs, S3, and other chip vendors, which bodes well for MoSys' future. We expect to see vigorous sales of the 1T-SRAM products as well, giving MoSys commercial success to go along with the technical advantages it has always had. M