MIPS RM7000 Emerges From QED

Two Levels of On-Chip Cache, L3 Cache Controller, Suit Chip for High End

by Jim Turley

Good things come to those who wait, and Silicon Graphics and some network OEMs have been waiting a long time for this one. One year behind schedule and two years after its initial announcement at the Microprocessor Forum (see MPR 10/28/96, p. 36), QED's RM7000 processor has emerged into the light of day.

The 300-MHz superscalar MIPS chip is part workstation processor and part high-end embedded processor. QED says it has a workstation customer, which could be SGI or a third-tier vendor like DeskStation. Most of the volume will come from networking equipment that will capitalize on the RM7000's big caches and high-speed bus interface.

The design is a logical extension of QED's philosophy: add value through cache and a high-speed pipeline, not with exotic design tricks. It's a sound strategy for a company with a small design team and access to good third-party foundries. The RM7000 is fast without veering into the RF realm (like Alpha), advanced without being too complex (like x86, SPARC, or PowerPC processors).

The part stands up well against other desktop chips that have slipped into the embedded realm, such as the PowerPC 603e and 604e, and other MIPS processors. It will appear in Lucent's PacketStar Access Server, among other products, before the end of this year.

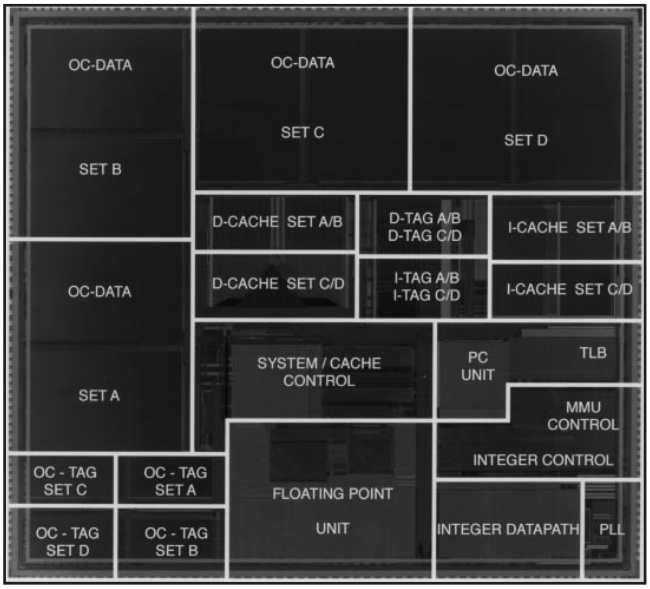

Figure 1. QED's RM7000 processor contains 15 million transistors in its 90 mm^2 of silicon. The chip is fabricated on IBM's 0.25-micron process.

Caches, Symmetric Core Set RM7000 Apart

The RM7000 is one of the few microprocessors in any category to integrate both L1 and L2 caches on the chip (the Alpha 21164, Exponential x704, and Intel's Mendocino being the others). The part's 16K instruction and data caches are backed with a unified 256K L2 cache. All three caches are four-way set-associative, write-back, and nonblocking, and all load the critical word first. For simplicity, replacement is by a cyclic rather than a least-recently-used algorithm.

As QED predicted nearly two years ago, the chip's 288K of cache is a record for any single chip. The caches take up about 60% of the RM7000's 90 mm^2 die, as Figure 1 shows.

Nonblocking caches—always a good idea—become even more vital in a superscalar processor. If one pipeline stalls due to a cache miss, the other can keep running by virtue of the RM7000's out-of-order execution.

That superscalar capability is the RM7000's biggest difference from its predecessors. The RM5230, '60, and '70 can execute two instructions per clock only if one is an integer instruction and the other is an FP operation. The RM7000's more useful configuration allows any two instructions to be dispatched together. QED's estimates put performance at 12–14 SPECint95 and 14–16 SPECfp95 (at 300 MHz with 1M of L3 cache), which is in the same integer range as the 13/10 rating of a 350-MHz Pentium II. The more mundane Dhrystone comes in at around 500 MIPS at 300 MHz, although this is an estimate, too.

If workstation-level performance seems uncompelling, QED's price difference makes up for it. The RM7000 isn't cheap, but its price/performance is top-notch. Starting at $150 for the 200-MHz chip, the price of the fastest (300-MHz) chip is—take a breath—$225. That works out to about $17 per SPECint95 and $15 per SPECfp95, versus $47/$55 for the 350-MHz 604e, and $30/$42 for Pentium II-350. This is the kind of trend embedded designers like to see, adding currency to the theory of trickle-down technology.

By the time Intel's Mendocino (Celeron) processor hits the streets in 3Q98, it may become the RM7000's stiffest competitor. Mendocino should approach the integer performance (but have half the SPECfp95 score) of the QED part and sell for around $130. That kind of price/performance persuaded SGI to give up MIPS for Intel chips.

Bus, Socket Match Earlier QED Parts

As promised, the RM7000 has the same bus as the RM5360 and RM5270 processors, so designers can reuse their PCB layout and/or logic designs. As this chip's schedule dragged out, QED aggressively pushed the RM5260 and '70 as placeholders for the RM7000.

The external cache interface doesn't change between the RM52xx chips and the new RM7000, even though the latter controls a tertiary (L3) cache instead of an L2 cache. Obviously, the L3 cache is optional; customers who are satisfied with the chip's performance using two levels of on-chip cache can run the RM7000 with no external cache.

The RM7000 has a higher maximum clock rate than its predecessors, but its greater selection of bus-clock divider ratios means that timid designers need not be reticent about using a 300-MHz processor. Those unacquainted with the delights of high-speed design need not deal with anything faster than 33 MHz. Bolder bandwidth barons can run the bus at up to half the CPU speed or 125 MHz, whichever is lower.

Interrupt handling has been enhanced to cater to embedded designers. Programmers can now set the spacing, or "stride," between interrupt vectors, from 0 to 512 bytes. Wide spacing allows the actual interrupt-service routine to take the place of the vector, while close spacing is for a more traditional jump table. Setting the spacing to zero effectively routes all interrupts to a single vector or ISR.

A Better Value Than PowerPC 603e, 604e

The RM7000 competes in the rarefied realm of high-end, 300-MHz embedded processors currently inhabited by only the MIPS, PowerPC, and Pentium parts listed in Table 1.

Motorola (and, to a lesser extent, IBM) has been diligent in discounting its PowerPC line. The 300-MHz EC603e (see MPR 6/22/98, p. 11) sells for just $109, so for basic networking applications—most of which don't need an FPU—the EC603e is a good value. The nondefective PowerPC 603e sells for $135 at 300 MHz, making it $90, or 40%, cheaper than the QED device. That $90 is more than enough for 256K of SRAM for the missing L2 cache, but it won't make up for the 603e's more restrictive superscalar issue model.

Compared with the 603e, the RM7000 gives you more grunt for your guilder. While the midrange PowerPC can dispatch one integer and one floating-point operation (and, potentially, one "folded" branch) per cycle, it can't perform the more common function of dispatching two integer operations side by side, as the RM7000 does.

The (much) more expensive PowerPC 604e can go toe-to-toe with the RM7000 on superscalar, floating-point, and bandwidth grounds, but at $500 and up for the faster parts, it gets pounded on price/performance.

NEC VR5464 Trades FP for Vector Performance

If MIPS compatibility is important, NEC's newly minted VR5464 (see MPR 3/9/89, p. 1) makes a strong claim for designers' attentions. At just $95, the VR5464 is dirt cheap in comparison to the RM7000. At 250 MHz, the NEC chip is $70 cheaper than the QED chip at the same speed. The VR5464 can dispatch two integer ops at once, or two FP ops at once (or an integer/FP with a vector operation).

The VR5464's most distinguishing characteristic is its vector-media unit, something none of its competitors currently offer. The hang-up is VR5464's floating-point performance, which belongs in the same rank as Pentium's. Designers with a yen for image processing should choose NEC; for conventional floating-point code, the RM7000 is closer to the mark.

	QED RM7000	NEC VR5464	Intel Pentium II	Motorola 604e	Motorola 750
Frequency	300 MHz	250 MHz	350 MHz	350 MHz	300 MHz
I/D Cache	16K/16K	32K/32K	16K/16K	32K/32K	32K/32K
L2 Cache	256K	None	512K	None	None
SPEC95b	13/15†	10/4.5†	13.8/10	14/12	13/8
Bus Speed	125 MHz	125 MHz	100 MHz	125 MHz	100 MHz
Power (typ)	n/a	4.4 W	13 W*	7 W	5 W
Available	4Q98	3Q98	Now	Now	Now
Price (1k)	$250*	$100*	$423	$600	$400

Table 1. QED's RM7000 stacks up well against other MIPS, PowerPC, and x86 processors. (Source: vendors except *MDR estimates; †vendor estimates)

The NEC chip has bigger primary caches, which impart some of the advantage of the RM7000's big L2 cache. Production schedules are comparable, with volume parts flowing later this year. The NEC chip draws about half the power of the QED device, partly because it's about half the size: just 47 mm^2 in a similar 0.25-micron process, a substantial size (and therefore, cost) advantage for NEC. The RM7000's extra 38 mm^2 go straight to its L2 cache, which pays dividends for some customers.

FPU Is Superfluous, But Bandwidth Is Tops

Network types are crazy for cache, which affects the performance of table lookups common within routers. Lucent has already announced its intent to use the RM7000 in some of its routers. Cisco uses QED's RM5270 in its equipment now, so an upgrade to the RM7000 seems a likely outcome there. Both makers will probably attach large L3 caches to get the most of the RM7000's abilities.

Fast transactions and big cache reserves: that's what the RM7000 offers. For makers of network boxes, QED is delivering a good combination of assets for growth. Compute-intensive applications might be better (or more economically) served by chips like the VR5464, but for moving data from Point A to Point B, with a little massaging in between, the RM7000 is right on the money. M

Price & Availability

The RM7000 is sampling now at 200, 250, 266, and 300 MHz. Production is scheduled for 4Q98. In 10,000-unit quantities, the chip is priced at $150, $165, $185, and $225 at each clock speed.

For more information, contact QED (Santa Clara, Calif.) at *www.qedinc.com/prod_web1.htm* or call the company at 408.565.0377.