by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send e-mail to belgard@umunhum.stanford.edu *with comments or questions.*

5,717,881

Data processing system for processing one- and two- parcel instructions
Issued: February 10, 1998
Inventors: Douglas R. Beard, et al
Assignee: Cray
Filed: June 7, 1995
Claims: 1
In a hardwired supercomputer with fixed-length instructions of n bits or 2n bits, a decoder that detects and issues, in a single cycle, a 2n-bit-sized instruction or issues the first of two n-bit instructions in that cycle and the second n-bit instruction in the next cycle.

5,715,425

Apparatus and method for prefetching data into an external cache
Issued: February 3, 1998
Inventors: Gary S. Goldman, et al
Assignee: Sun
Filed: February 22, 1996
Claims: 13
A FIFO load buffer connected between a processor cache and external memory. The FIFO load buffer issues a load request to external memory on a data-prefetch instruction from the instruction stream. The buffer also generates the external memory request required for an access to memory on a cache miss, but does so during the load latency of any prefetch request.

5,712,997

System and method for processing load instruction in accordance with "no-fault" processing facility, including arrangement for preserving access fault indicia
Issued: January 27, 1998
Inventor: David Dice
Assignee: Sun
Filed: January 31, 1996
Claims: 32
A microprocessor and methods such that a load instruction, whose execution causes a fault, sets a flag in the associated target register of the load.

5,712,972

Identification of faults in data paths and functional units of a central processing unit by a systematic execution of test instructions
Issued: January 27, 1998
Inventor: Sunil Kakkar
Assignee: Sony
Filed: June 7, 1995
Claims: 21
A systematically structured diagnostic for detecting, isolating, analyzing, and reporting problems or faults in a CPU. The diagnostic causes the CPU to execute instructions selected, such that the CPU must use every data path and functional unit. Errors caused by particular instructions are correlated with the functional units or data paths.

5,710,936

System resource conflict resolution method
Issued: January 20, 1998
Inventors: Patrick J. Meaney, et al
Assignee: IBM
Filed: June 7, 1995
Claims: 5
A method for establishing priority of functional resources in a processor. The method uses a register. The register contains a bitmap of the current usage of the resources. Operations in the pipeline each generate a bitmap indicating their resource requests in a queue. Pipeline priority is given to a queue entry with no resource conflicts. The register is updated to reflect the resources used by the operation chosen from the queue.

5,710,929

Multistate power management for computer systems
Issued: January 20, 1998
Inventor: Henry Tat-Sang Fung
Assignee: Vadem
Filed: June 2, 1995
Claims: 12
Power-conservation system that monitors the activity of the system. The system has multiple modes of conservation. Coupling of circuit power and clock signals is used to control power consumption, and both hardware and software components may monitor and control operations separately or together.

OTHER ISSUED PATENTS

5,715,440 *Branch-instruction-executing device for tracing branch instruments based on instruction type*
5,710,933 *System-resource-enable apparatus*