by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send e-mail to belgard@umunhum.stanford.edu *with comments or questions.*

5,737,561

Method and apparatus for executing an instruction with multiple branching options in one cycle
Issued: April 7, 1998
Inventor: Carole DuLong
Assignee: Intel
Filed: November 1, 1996
Claims: 9
A CASE instruction is disclosed. The CASE instruction uses an encoding to select condition bits of the processor whose binary values, concatenated, select one of *n* registers that have been preloaded with appropriate target destination addresses. The CASE instruction "decodes" the selected condition bits to choose the register with the target address corresponding to the processor state, transferring control to the address in that register in a single cycle.

5,737,550

Cache-memory to processor-bus interface and method thereof
Issued: April 7, 1998
Inventor: Seungtaik Michael Song
Assignee: AMD
Filed: March 28, 1995
Claims: 24
A method and system for compatibly emulating external cache-fill bus-burst behavior of a microprocessor (e.g., a Pentium-like processor) with a microprocessor that has a cache-line size less than that of the emulated microprocessor. The system or method emulates the cache-fill bus burst of the emulated microprocessor, but it transfers to the cache only the native cache-line-size data. The remainder of the data is buffered in the bus-interface unit in the event that it is actually referenced.

5,737,548

RISC-based microcontroller with peripheral function added to a split data bus
Issued: April 7, 1998
Inventors: Randy L. Yach, et al
Filed: November 7, 1995
Claims: 8
A RISC-based microcontroller that uses "split" data buses in the ALU and I/O peripheral control interface. The microprocessor writes data on the bus during positive clock edges and reads data during negative clock edges.

5,734,881

Detecting short branches in a prefetch buffer using target location information in a branch target cache
Issued: March 31, 1998
Inventors: Christopher E. White, et al
Assignee: Cyrix (National)
Filed: December 15, 1995
Claims: 25
A pipelined processor includes a prefetch buffer and a branch unit that cooperate to detect when the target of a branch (a "short branch") is already in the prefetch buffer, thereby avoiding issuing a prefetch request to retrieve the target.

5,734,879

Saturation instruction in a data processor
Issued: March 31, 1998
Inventors: Michael G. Gallup, et al
Assignee: Motorola
Filed: March 22, 1995
Claims: 17
A processor that executes instructions on vector ("MMX-like") instructions. A first instruction calculates results and overflows for vector elements of the data. A second instruction saturates the vector elements on the basis of overflows stored by the first instruction execution.

5,732,242

Consistently specifying way destinations through prefetching hints
Issued: March 3, 1998
Inventor: Todd C. Mowry
Assignee: Silicon Graphics
Filed: March 24, 1995
Claims: 20
A processor with an n-way cache that executes data prefetch instructions containing hint fields. The hint fields contain a part that enables cache "way selection" and a part that specifies the way to be selected. The prefetch instruction also contains an address. When the hint field specifies way selection, the appropriate cache line way, selected by the way part of the hint field, is selected for refill.

OTHER ISSUED PATENTS

5,734,854 *Fast instruction decoding in a pipeline processor*
5,732,254 *Pipeline system branch-history table storing branch instruction addresses and target addresses with inhibit bits*
5,732,253 *Branch processing unit with target cache-storing history for predicted taken branches and history cache-storing history for predicted not-taken branches*
5,732,243 *Branch processing unit with target cache using low/high banking to support split prefetching* M