## VIA, S3 Get P6-Bus Licenses

Intel has opened the door for other vendors to build devices that connect directly to the processor bus in Celeron and Pentium II systems. After implicitly threatening vendors that were considering selling products for the P6 bus, Intel has chosen to license that bus to two key players: chip-set maker VIA Technologies and graphics vendor S3. Each licensee is the second-largest vendor in its respective market.

VIA *(www.via.com.tw)* needed the license to continue to supply chip sets to the PC market. With Intel no longer shipping desktop Socket 7 processors, VIA has been limited to selling chip sets for systems using only non-Intel processors. With the Socket 7 market likely to disappear over the next year or two, VIA needed to move to the more popular P6 bus.

Ironically, the Taiwanese vendor was the first company apart from Intel to announce a P6-bus chip set (see MPR 2/12/96, p. 6), but it never shipped that product. Earlier this year, VIA announced another P6-bus chip set, the Apollo Pro, but said it would use an Intel-licensed foundry to build the chips. The new agreement allows VIA to use any foundry, without legal threat from Intel.

The Apollo Pro (see MPR 6/1/98, p. 26) is a traditional chip set similar to Intel's 440BX. In addition, VIA is pursuing a strategy of integrating graphics into the north bridge of its chip sets, starting with its recent Apollo MVP4 (see MPR 8/24/98, p. 4). We expect the company to soon deploy a similarly integrated product for the P6 bus.

With its new license, S3 plans to produce its own north-bridge/graphics chips based on its popular graphics accelerators. The company must develop or license a north-bridge design to complete such products. S3 needs an integrated product to compete against Intel's forthcoming Whitney chip set, which combines a version of Intel's 740 graphics core with its 440EX north bridge, and VIA's chips.

Intel isn't giving away its P6-bus technology for free. VIA provided Intel with access to its patent portfolio, which is fairly limited, and also agreed to pay Intel royalties on P6-bus devices. S3's agreement does not require such royalties, as it has a stronger patent portfolio that includes the notorious Exponential patents (see MPR 2/16/98, p. 5), which appear to cover aspects of Intel's Merced design. By cross-licensing with S3, Intel gains another P6-bus partner and eliminates the possibility of a patent lawsuit that would disrupt the Merced launch.

More deals are in the works, but Intel will continue to require some value in exchange. There is no shortage of takers. Chip-set maker SiS has already developed its own unlicensed P6-bus chip set (see MPR 9/14/98, p. 15), and other chip-set vendors face the same Socket 7 dilemma. Other graphics-chip makers must find a way to compete with integrated products from Intel, S3, VIA, and others. A P6-bus license will soon be required to be in the low-cost graphics market. —*L.G.*

## S3 Jumps on UMC's 0.18-Micron Process

S3 is readying its next-generation 3D-graphics chip, which the company says will have higher performance than its current Savage3D chip. Although it expects the new chip to operate at much lower power and have many new features, S3 is not disclosing details about the chip at this time, other than to say the nine-million-logic-transistor part will be built in a 0.18-micron process—unusually aggressive for a 3D chip. S3 plans to begin production of the new part in 2Q99.

Initially, the S3 chip will be built in UMC's 0.22-micron five-layer-metal process, which has about 10% smaller interconnect features than its 0.25-micron process and is outfitted with 0.18-micron transistors. During 2H99, the chip will move into UMC's true 0.18-micron L180 process, giving it a small frequency boost and about 30% reduction in die size.

L180 is a 1.8-V process that can have up to six layers of aluminum interconnect. The process parameters UMC has disclosed place L180 ahead of IBM's 0.22-micron CMOS-7S (see MPR 9/14/98, p. 1) and only slightly behind IBM's 0.18-micron CMOS-8S, which will enter production at about the same time. Thus, the L180 process puts UMC ahead of other pure foundries, which have historically lagged microprocessor vendors by a year or more. UMC has licensed copper-interconnect technology from IBM and plans to upgrade L180 to copper for volume production in 4Q99.

S3's new part will be one of the first 3D chips rendered in a process similar to that used for high-end microprocessors. Most previous 3D parts have, for cost reasons, used prior-generation technology, but the highly competitive 3D market is forcing vendors to pull every performance lever to eke out an advantage. While S3 may be the first to pull the 0.18-micron lever, others are sure to follow. S3 is fortunate to have a foundry with such aggressive process plans. In 1998, UMC spent more than a billion U.S. dollars on R&D and fab capacity, fourth among semiconductor vendors behind Intel, Motorola, and Siemens. It plans to repeat this spending level in 1999.

UMC says the S3 part is the beginning of a trend. It expects 3D chips to become process drivers, rather than followers, matching microprocessors micron for micron. Although this sounds good, it's not easy in practice. Leading-edge technology has costs. Early in the life cycle, wafer costs can be high and yields low. Although the several-hundred-dollar processors Intel builds by the millions can cover the premium, the same may not be true for 3D chips. Current 3D chips, while having die sizes as large as or larger than high-end microprocessors, typically sell for only a tenth the price. It is not clear whether the volume 3D market will bear a higher price, even for higher performance. But assuming UMC's new process is cost-effective, it could boost S3 into the performance lead—at least for a while. —*K.D.*

## Sun Grinds Out New Sparcs

Delivering on the roadmap it rolled out in September (see MPR 10/5/98, p. 15), Sun Microsystems has announced the availability of three new speed grades for its UltraSparc-2 and UltraSparc-2i processors.

The US-2, previously available at up to 360 MHz, is now shipping at 400 MHz and will be accelerate to 450 MHz in the spring. Although the 400-MHz version was anticipated, Sun's roadmap did not call for higher frequencies until mid-1999, when the 480-MHz US-2 was scheduled to ship. Sun says the 480-MHz version is still planned and on schedule. The 400-MHz US-2 delivers 14.0 SPECint95 (base) and 25.7 SPECfp95 (base) performance, roughly 10% and 5% speedups over the previous 360-MHz parts. The 400-MHz US-2 processors with 4M of cache list for $4,249 (1,000 units); pricing for 450-MHz modules was not announced.

Also according to plan, Sun is upping the top speed of its integrated US-2i line from 333 MHz to 360, boosting integer and floating-point performance by about 5%. A 360-MHz module with 2M of cache sells for $1,400. —*K.D.*

## Siemens Announces First TriCore DSP

At the recent Embedded Processor Forum, Siemens revealed that it has fabricated the first implementation of its hybrid DSP/microcontroller architecture, TriCore. Siemens' Rod Fleck explained that the initial test chips will be used to validate the TriCore architecture (see MPR 11/17/97, p. 13) and debug TriCore development tools.

The current TriCore chips execute at only 33 MHz at 3.3 V in Siemens' 0.35-micron three-layer-metal CMOS process with embedded DRAM. Siemens is hopeful future devices will reach 80 MHz by the middle of 1999 in its 0.25-micron process. DSP benchmark results from BDTI suggest that if Siemens achieves its 80-MHz target clock rate, TriCore's DSP performance will be comparable to that of current mainstream DSPs such as TI's TMS320C54x. TriCore's code density on control-oriented code appears comparable to that of other hybrid DSP/microcontrollers such as Hitachi's SH-DSP.

The current chip may, however, be the last of its kind. Siemens has said that the architecture of all future TriCore implementations will be slightly enhanced over that used in the unnamed test chip. The test chip is thus likely to be the only implementation of the original TriCore architecture; the unspecified enhancements will give all future TriCore chips a superset of the features of the original test chip.

This abrupt update may be a reflection of Siemens' wish to get initial silicon out the door as quickly as possible, while final adjustments to the architecture are still in progress. At Embedded Processor Forum, Siemens' Fleck hinted that the roadmap for TriCore might include a floating-point version. —*Jennifer Eyre, BDTI* M