Intel, Analog Devices Team for DSPs

Intel and Analog Devices (ADI) announced the formation of a joint effort to develop a next-generation DSP architecture targeting embedded applications. The surprise move echoes last year's debut of StarCore, the Motorola/Lucent partnership for DSP-core development. Intel and ADI will open a joint engineering center in Austin, building on teams that both companies currently have in place there.

Although ADI and Intel executives studiously avoided providing details about the design they plan to produce, they did state that they will develop a moderate-performance fixed-point architecture targeting cost- and energy-conscious embedded applications. The new architecture will be incompatible with existing devices and will target emerging communications applications and Internet appliances.

This suggests that the new architecture will succeed ADI's ADSP-21xx family. The '21xx has garnered design wins in a wide variety of audio, telecommunications, and industrial applications, largely by virtue of its relatively benign programming model and the availability of a wide range of choices in on-chip memory and peripherals. But the architecture is ancient, and ADI has been unable to match the performance of competing high-volume devices. ADI's recently announced Hammerhead and TigerSHARC architectures, in contrast, are high-performance designs aimed at lower-volume applications, where cost and power consumption are less critical. At a time when ADI is already preoccupied with deploying these two new high-end families, ADI expects that the Intel partnership will enable it to launch the new low-cost fixed-point architecture much faster than if it were working alone.

For Intel, partnering with ADI provides an opportunity to leverage the application know-how and market credibility of an established DSP-chip vendor. By adopting a common architecture, both companies hope to attract strong support from third-party tool providers, application-software vendors, and other development-infrastructure providers. This kind of support is increasingly vital as DSP applications become more complex and ubiquitous. Indeed, strong third-party support has been a key factor in enabling market-share leader Texas Instruments to sustain its dominance in DSPs. In addition to third-party support, Intel and ADI will jointly develop some tools and application software for the new architecture.

As with all such partnerships, it remains to be seen whether these two large, established companies can collaborate effectively on developing a new architecture—particularly given the likelihood that they will ultimately compete with each other by selling chips based on a common core. The value of the partnership will remain an open question until it begins to bear fruit. According to the partners, the first core design implementing their new architecture will emerge some time next year. —*Jeff Bier, BDTI*

Philips Exits PDA-Processor Biz

Philips Semiconductor has quietly made a strategic exit from the business of making microprocessors for handheld organizers, PDAs, and palm-size PCs. The company's TwoChip PIC processor (PR31700; see MPR 5/12/97, p. 13), used in Philips's own Velo and Nino Windows CE units, is effectively orphaned, with no offspring in sight.

Philips will instead focus its development efforts on mixed-signal companion chips for embedded processors, such as its successful UCB1100 and UCB1200 chips. These chips provide the analog/digital interface required for touch-screen, speaker, and modem functions common to handheld systems. Philips felt that its line of MIPS-based processors provided little differentiation from similar devices from Toshiba, NEC, and others. Indeed, Philips's short-lived series of PDA processors was based on Toshiba core designs.

Philips will remain active with its MIPS license (the company, like most others, also has an ARM license), building MIPS-based processors for TV set-top boxes and similar systems. Philips will also develop companion devices for standalone MIPS chips in the R5000 class. Windows CE–based palm-sized PCs have not been particularly successful in the market, lagging behind the leading units from 3Com (Palm) and Psion. Dividing the WinCE market share among six or more vendors only makes matters worse. It appears that Philips bowed to the inevitable, shunting its development staff to more distinct product lines, leaving the CPU development in more experienced hands. —*J.T.*

EEMBC Sells Benchmarks, Opens Testing Lab

The EEMBC benchmark group (see MPR 4/20/98, p. 13) is making its suite of embedded benchmark code available to nonmembers. Any interested party can now license the benchmark suite for a one-time fee of $30,000, with $5,000 annual renewal fees ensuring regular updates. Previously, the EEMBC tests were available only to the group's 24 members, which are exclusively microprocessor vendors.

At the same time, the nonprofit consortium founded ECL, the EEMBC Certification Labs, a for-profit business to certify the results of all benchmark testing. EEMBC bylaws prohibit the publication of benchmark results until (or unless) they have been verified by ECL. ECL's customers will be EEMBC members that call upon the lab to "bless" results deemed worthy of publication. Presumably, vendors with poorly performing chips would have no incentive to pay for ECL's services.

By licensing its benchmarks to nonmembers, the EEMBC hopes to attract compiler vendors, operating-system makers, and hardware OEMs that wish to tune their products to perform better on the tests. Compiler writers have historically tweaked their wares in order to produce

better benchmark scores, a philosophy that runs somewhat counter to the spirit of the benchmark. Nevertheless, the wider distribution of EEMBC's code should help to make it more popular and, therefore, more useful as a metric for comparison. —*J.T.*

Galileo Announces System Logic for PowerPC

Galileo Technology (*www.galileot.com*) has extended its line of a half-dozen system-logic chips for MIPS processors with a new pair for PowerPC chips. The GT-64130 and '131 are similar to Galileo's existing core-logic chips but work with the PowerPC 603e, 740, 750, and 860 series of processors from IBM and Motorola.

Both the '130 and the '131 include a 64-bit SDRAM interface, a DMA controller, I_2O-compatible interrupts, and one ('131) or two ('130) 32-bit, 66-MHz PCI buses. On the '130, the two PCI interfaces may be ganged to create a single 64-bit interface. The so-called Universal PCI interfaces accept both 3.3-V and 5-V logic levels and comply with CompactPCI hot-swap requirements.

Galileo's two new products move it into competition with PowerPC core-logic suppliers Tundra and V3. Tundra's QSpan and PowerSpan products (see MPR 10/5/98, p. 9) have a lead in the market among PowerPC users, while Galileo has a track record with MIPS customers. Galileo's prices of $54 ('131) and $65 ('130) are certainly higher than commodity PC chip-set prices but competitive for embedded systems, where there are few alternatives. —*J.T.*

IDT Debuts Two System-Logic Chips

After creating a new line of embedded MIPS processors, IDT is now rolling out core-logic chips to support them. The RC64145 and RC32134 are for 64-bit and 32-bit chips, respectively, and both include an SDRAM controller, PCI interface, multichannel DMA controller, timer, UARTs, parallel port, and interrupt logic. The major difference between the two chips is the width of their CPU bus: 64 bits for the 64145 and 32 bits for the 32134. The '145 also supports the faster 66-MHz PCI transactions.

More subtly, the 32-bit chip gates memory directly onto the host processor's data bus, while on the '145, data passes through the part. This is because the 64-bit SysAD bus, common to workstation-class MIPS CPUs, does not support data sizing, high-impedance signals, or variable slave timing. IDT's new 32364 processor bus, in contrast, was designed specifically to support these features, making it easier to integrate into typical embedded systems.

Samples of both core-logic chips are available now; production is in 2Q99. Prices are a reasonable $20 ('134) and $41 ('145) in 10,000-unit quantities. IDT's 64145 is a dead ringer for Galileo's GT-64120 but without I_2O support or the ability to split the PCI bus in half; at about $20 less expensive, that's a fair tradeoff in IDT's favor. —*J.T.* M