by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send e-mail to belgard@umunhum. stanford.edu with comments or questions.

5,774,737

Variable word length very long instruction word instruction processor with word length register or instruction number register
Issued: June 30, 1998; Filed: October 10, 1996
Inventor: Hiraku Nakano
Assignee: Matsushita
Claims: 49
In a VLIW processor, an instruction-length register is provided. VLIW instructions are fetched and decoded according to their length, as determined by the register. An operation is provided to alter the instruction-length register so subsequent VLIW instructions are fetched and decoded according to the new instruction length. Consequently, sparse VLIW instructions can be narrower, or different instruction sets may be processed.

5,774,704

Apparatus and method for dynamic central processing unit clock adjustment
Issued: June 30, 1998; Filed: July 30, 1996
Inventor: Ian Michael Williams
Assignee: Silicon Graphics
Claims: 28
In a computer system, a device to dynamically adjust a CPU clock. The device is composed of a clock-pulse generator and a controller. The clock-pulse generator generates the input to the CPU clock. The frequency is variable over a range. A controller is coupled to the clock-pulse generator for adjusting the frequency over the range. The controller adjusts the clock frequency such that the frequency increases when the load on the CPU increases and decreases when the load on the CPU decreases.

5,774,694

Method and apparatus for emulating status flag
Issued: June 30, 1998; Filed: September 25, 1996
Inventor: Srinivasan Murari
Assignee: Intel
Claims: 30
A method or apparatus for emulating status flags on a computer system that has no native support for status flags, particularly, the carry flag. The steps involve decoding an arithmetic instruction executable on a first (native) ISA, where, if executed on the native ISA, the instruction would generate at least one status flag. The instruction is translated to be executed on a second ISA. The translated instruction (executed on the second ISA) generates an intermediate result by XORing its two operands. A final result is achieved by XORing the intermediate result with the arithmetic result, generating at least one bit that is equivalent to the status flag.

5,774,686

Method and apparatus for providing two system architectures in a processor
Issued: June 30, 1998; Filed: June 7, 1995
Inventors: Gary Hammond, et al.
Assignee: Intel
Claims: 66
A processor having two system configurations is described. The processor includes an instruction-set unit, a system unit, an internal bus, and a bus unit. The system unit can operate in one of two modes, each mode providing a different system architecture. The instruction-set unit operates to provide execution of a first instruction set in one mode and a second instruction set in the other mode.

5,771,382

System and method for synchronizing static variable initialization and reference under a multi-threaded computer environment
Issued: June 23, 1998; Filed: August 14, 1997
Inventors: I-Shin Andy Wang et al.
Assignee: IBM
Claims: 12
System and method to avoid static-variable initialization and reference conflicts in a multithreaded computer system. A CPU makes a lock request on the locking thread to lock the static variable. In response, the system enters a single-thread mode. The locking thread operates on the static variable. Subsequently, the system may reenter multi-threaded mode.

5,770,894

Parallel processing method having arithmetical conditions code based instructions substituted for conventional branches
Issued: June 6, 1998; Filed: July 10, 1996
Inventor: Ramesh Chandra Agarwal
Assignee: IBM
Claims: 15
A system and methods whereby a superscalar processor performs arithmetic operations in lieu of conditional branches, primarily so loops can be unrolled. Condition codes are set based on the arithmetic operations, such as compare instructions. As a result of condition codes set by compare operations, additional arithmetic operations may be performed that select one (or both) of two compared operands on which to operate. The additional operations may be performed in parallel. Ⓜ