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# WinChip 2: Low-Price Leader

## *Enhanced IDT Processor Reaches 300 Performance Rating*

*by Michael Slater*

Nine months later than planned, IDT has begun volume shipments of WinChip 2, an enhanced version of the original C6 design created by the company's Centaur Technology subsidiary. WinChip 2 includes an entirely new floating-point unit, a dual-issue MMX unit, 3DNow, and enhanced TLBs and branch prediction. In addition, it supports a 100-MHz bus and fractional bus multipliers.

Unfortunately, the long delay in shipping WinChip 2 has prevented IDT from improving its performance position relative to its competitors'. IDT's fastest part now runs at 250 MHz and is performance-rated as WinChip 2-300 to indicate that its performance is comparable to that of its chief competitor, Cyrix's M II-300 (see Figure 1). Unlike the Cyrix part, WinChip 2 implements 3DNow; it is the first chip from a company other than AMD to do so. At $38, it is less expensive than Cyrix's already bargain-priced chip and outperforms it on floating-point and MMX functions.

### Fab Switch Delayed Shipment

IDT began shipping the original WinChip, its first x86 processor, in late 1997 (see MPR 6/2/97, p. 1). These shipments have been small, with about 850,000 processors delivered in 1998. With the new WinChip 2 and upcoming WinChip 3, IDT expects to ship more than two million chips in 1999.

The delays in the WinChip 2 is due primarily to a change in fabs. This chip is designed for IDT's most aggressive process, which was running only at IDT's 150-mm Fab 3 in San Jose. IDT decided to shut down this fab and use its new 200-mm Fab 4 in Hillsboro, Oregon, but Fab 4 was not yet running the new process. As often happens, bringing up a new process in a new fab took longer than anyone had expected. IDT says these hurdles are now behind it, and that WinChip 2 will be in full production in April.

IDT entered into a foundry agreement with IBM in early 1998 but chose not to build chips there right away. IDT plans to build WinChip 2 and WinChip 3 in its own fab and use IBM for WinChip 4.

### New FPU, MMX, 3DNow Units

WinChip 2 includes an entirely new floating-point unit that is fully pipelined, except for double-precision multiplies. This puts it well ahead of Cyrix's M II on FP code, though it is slower than Celeron. Compared with AMD's K6 family, WinChip 2 has a higher FP issue rate but longer latencies.

WinChip's original MMX unit was also replaced. The new design is able to execute two MMX instructions per cycle. The 3DNow unit also executes two instructions per cycle. For standard integer code, however, WinChip 2 is a scalar processor, like the original WinChip.

As first described at Microprocessor Forum in October 1997, WinChip 2 was slated to implement a proprietary set of 3D instruction-set extensions (see MPR 11/17/97, p. 17). Early in 1998, Centaur came to an agreement with AMD and Cyrix on 3DNow, and it changed its design to be compatible with

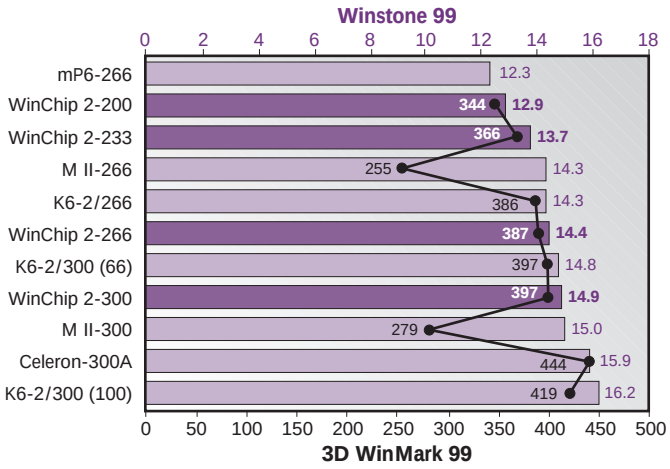


**Figure 1.** WinChip 2 compares well with its chief competitor, Cyrix's M II, especially on the 3D benchmark. All tests were run under Windows 98 with DirectX 6.0. The Celeron system used an Asus P2L-B motherboard with an Intel 440LX chip set. All others used a Gigabyte 5AX motherboard with an ALi Aladdin V chip set and 512K L2 cache. All have 64M of PC100 SDRAM, a 4.3G Western Digital hard drive, and a Diamond V550 AGP graphics card. (Source: ZDTag performance report, commissioned by IDT.)

that standard. WinChip 2 matches the K6-2's 3DNow performance (based on instruction-cycle counts) for all instructions except reciprocal square root, which takes two cycles on the K6-2 but 10 cycles on WinChip 2 (see MPR 6/1/98, p. 1). This compromise was made to keep the die size down.

A less visible addition to the original WinChip is branch prediction, which was entirely omitted in the original design. WinChip 2 has a 4K-entry branch-history table with one bit per entry that predicts the direction of each branch. The chip does not cache target addresses. It uses a two-level indexing method known as Gshare and an encoding method called "agrees" (see MPR 11/17/97, p. 22).

Centaur made several other small improvements to the WinChip design. The TLB size was doubled to 128 entries, the data cache was made four-way set-associative instead of two-way, and the speed of several instructions (notably integer multiply) was increased by one or more clock cycles.

Despite the additions in WinChip 2, its die size remains impressively small: the six-million-transistor device occupies only 58 $mm^2$ in IDT's 0.25-micron five-layer-metal process, making it the smallest x86 PC processor in production today. In a 296-pin PGA, the MDR Cost Model estimates the manufacturing cost to be $25.

As Table 1 shows, IDT will offer WinChip 2 in both a conventional Socket 7 PGA and in a BGA package. The BGA version uses a slightly different die; it is the first split-rail WinChip and has a 2.8-V core. This low-power version, which is limited to the 200 and 233 speed grades, is intended for very low cost PCs, PC processor upgrades, and embedded applications. (IDT plans to attack the notebook computer market with the faster WinChip 3.)

## Clock Speed Still Limited

One metric in which WinChip 2 improves little on its predecessor is clock speed. The original WinChip's top clock speed is 240 MHz. Because it does not support fractional bus multipliers, however, this speed requires a slow 60-MHz bus, and the chip does not support the common 233-MHz core speed.

WinChip 2 boosts the maximum clock speed to only 250 MHz, but by running the bus at 100 MHz (along with the TLB, branch prediction, and other enhancements described above) it delivers significantly higher performance, even on code that does not benefit from the faster FP and MMX units or the 3DNow capability.

The delays in ramping up production of WinChip 2 provided time for Centaur to revise the design to support not only the conventional one-half bus multipliers (3.5, 4.5, etc.) but also one-third multipliers (such as 2.33). This allows the company to offer a 233-MHz chip with a 100-MHz bus. Because this chip outperforms other 233-MHz parts, which must use a 66-MHz bus, IDT decided to label the part as the WinChip 2-266. As with Cyrix's M II and Rise's mP6, the suffix indicates the performance rating, not the clock speed. The fastest version, which will not be available in volume until June, uses a 250-MHz CPU and a 100-MHz bus; it is sold as the WinChip 2-300. IDT also offers 200- and 233-MHz speed grades with a 66-MHz bus; these parts are not performance-rated, since they do not have the benefit of the faster bus.

As Figure 1 shows, the performance ratings hold up well (according to ZDTag's testing, as commissioned by IDT) against Cyrix's M II and Rise's mP6 as well as AMD's K6-2 configurations with a 66-MHz bus, based on the Business Winstone 99 benchmark running under Windows 98. Some K6-2/300 systems use a 100-MHz bus, and those systems outperform the WinChip 2-300 by nearly 9%. Intel's Celeron-300A beats the WinChip 2-300 by about 7%. (The WinChip 2-300 would fare well against the original Celeron-300, which had no L2 cache, but that part is now gone from the market.)

Thus, IDT's ratings overstate performance by roughly one speed grade relative to Celeron systems or AMD K6-2 systems with a 100-MHz bus. Since Cyrix's ratings fall short by a similar amount, and Cyrix is the company's most important competitor, IDT felt it necessary to rate its part on the same diluted scale used by Cyrix. In essence, the performance-rating scale has slid down, confusing the meaning of the ratings. Performance ratings, once formally defined as delivering performance within ±1.5% of the equivalent Intel chip, are now defined with as much as 10% leeway—larger than the gap between adjacent speed grades in many cases.

While it is discouraging to see the performance-rating scheme become watered down, IDT's decision is understandable, considering the lack of Intel parts as alter-

| | Speed Grade | Core Speed | Bus Speed | Core Voltage | Typical Power | Samples | Production |
|---|---|---|---|---|---|---|---|
| WinChip 2 | 200 | 200 MHz | 66 MHz | 3.3, 3.52 | 7.3 W | Now | April |
| | 233 | 233 MHz | 66 MHz | 3.3, 3.52 | 8.5 W | Now | April |
| | 266 | 233 MHz | 100 MHz | 3.52 V | 9.0 W | Now | April |
| | 300 | 250 MHz | 100 MHz | 3.52 V | 9.7 W | Now | June |
| WinChip 2 BGA | 200 | 200 MHz | 66 MHz | 2.8 V | 4.6 W | April | July |
| | 233 | 200 MHz | 100 MHz | 2.8 V | 5.4 W | April | July |
| WinChip 3 | 266 | 233 MHz | 66 MHz | 2.8 V | 7 W | April | August |
| | 300 | 266 MHz | 66 MHz | 2.8 V | 8 W | April | August |
| | 333 | 266 MHz | 100 MHz | 2.8 V | 8 W | April | August |
| Mobile WinChip 3 | 233 | 200 MHz | 66 MHz | 2.2 V | 3 W | April | August |
| | 266 | 233 MHz | 66 MHz | 2.5 V | 5 W | April | August |
| | 300 | 266 MHz | 66 MHz | 2.8 V | 8 W | April | August |
| | 333 | 266 MHz | 100 MHz | 2.8 V | 8 W | April | August |
| WinChip 4 | 400 | 400 MHz | 100 MHz | 2.8 V | 14 W | 3Q99 | 4Q99 |
| | 450 | 450 MHz | 100 MHz | 2.8 V | 16 W | 4Q99 | 1Q00 |
| | 500 | 500 MHz | 100 MHz | 2.8 V | 18 W | 1Q00 | 2Q00 |
| Mobile WinChip 4 | 400 | 400 MHz | 100 MHz | 2.2 V | 9 W | 1Q00 | 2Q00 |

**Table 1.** IDT's WinChip 2 will be followed quickly by WinChip 3, with WinChip 4 joining by the end of the year. (Source: IDT)

native points of reference. For IDT to rate its 250-MHz chip as a 266 speed grade would be giving too much away, since it is faster than either a Pentium/MMX-266 or a Celeron-266 (which had no L2 cache).

According to 3D WinBench, WinChip 2 delivers 3D graphics performance comparable to that of AMD's K6-2 with a 66-MHz bus. The WinChip 2-300 falls 5% behind a K6-2/300 with a 100-MHz bus and 11% behind a Celeron-300A. For both the IDT and the AMD parts, these tests use 3DNow code in Microsoft's DirectX 6 software. Celeron, with its faster L2 cache and better FP performance, achieves the best performance, even without 3D extensions. The M II, with its slow FP and no 3D extensions, falls far short; the M II-300 is 30% slower than the WinChip 2-300.

The mP6, from upstart competitor Rise (see MPR 11/16/98, p. 1), performs poorly. Rise has positioned its chip against the original WinChip, and IDT's enhancements appear to leave Rise far behind. Rise's 200-MHz part, which the company rates as a 266 speed grade, is 15% slower than the 233-MHz WinChip 2-266 and slower than even the 200-MHz WinChip 2. Surprisingly, ZDTag was unable to get the Rise chip to complete the 3D test.

## Next Up: WinChip 3

IDT doesn't plan to rest on WinChip 2 for long: samples of WinChip 3 are promised for April, with production in August. This chip is identical to its predecessor, except that the L1 cache size is doubled to 128K. According to IDT's measurements, the increased L1 cache size delivers an 8–10% performance boost. With the larger cache, WinChip 3 can reach the 300 performance point without a 100-MHz bus; the WinChip 3-300 will use a 266-MHz core and a 66-MHz bus. The WinChip 3-333 will be the top speed grade, also running at 266 MHz internally but with a 100-MHz bus.

The 10.2-million-transistor WinChip 3 is only modestly larger, at 76 $mm^2$, yielding an estimated manufacturing cost of $30. IDT plans to offer mobile versions as well. IDT's designs are well tuned for low power, but the company's process can't run at the low supply voltages used by its competitors, holding the chips back in the mobile arena. IDT plans to offer WinChip 3 in both PGA and BGA packages, as well as in an Intel-compatible mobile module—which would be the first non-Intel mobile module.

## WinChip 4 To Break Speed Barrier

After being stuck at top speeds of 240 to 266 MHz for its entire history, IDT expects to break into a higher-speed category with the WinChip 4 (see MPR 12/7/98, p. 18), which it will build initially at IBM. This new core design uses a much deeper pipeline to enable higher clock speeds. IDT expects to sample this chip at 400 MHz in 3Q99, with production in 4Q99. Production at 450 MHz is planned for 1Q00, with 500 MHz in 2Q00. The 11.6-million-transistor chip measures 115 $mm^2$—rather portly for an IDT chip, in part because of the IBM process IDT is using—and presumably will be moved into a denser process before it reaches its peak volume. In a 0.18-micron process, it could hit 650 MHz by the end of 2000.

IDT plans to ship a mobile version of WinChip 4 running at 400 MHz in 2Q00. All the WinChip 4 parts will use a 100-MHz bus and will be sold based on clock speed, not on a performance rating.

### Price & Availability

WinChip 2 will be in volume production in April, except for the top speed grade, which is due in July (see Table 1 for availability of other products). Pricing is $30, $35, and $38 for the 200, 233, and 266 speed grades in quantities of 5,000; pricing for the 300 speed grade has not been announced.

For more information, access *www.winchip.com*.

## Finding Profits at the Low End

Given its performance position, IDT doesn't expect to earn premium prices. At only $30 in thousands, the 200-MHz version is the least expensive PC processor available. IDT hasn't yet announced pricing for the WinChip 2-300, but the company has consistently priced its chips below Cyrix's; the M II-300 currently lists for $46.

IDT's ability to hit the 300 grade is essential, since PCs at speeds lower than this are rapidly disappearing. Before long, the 300 grade will be gone as well. Because its speed grades will continue to fall below the bottom end of Intel's roadmap, WinChip 2 is likely to find little success in the U.S. market. In developing countries, however, where any PC is a great advance over none at all, the slower-grade chips are still acceptable; after all, these chips would have been considered hot processors just two years ago. In these developing markets, a $20 saving in processor price is more important than a 20% boost in performance.

With WinChip 3, IDT may find some success in entry-level notebooks. It is not until the debut of WinChip 4, however, that IDT appears to have a shot at even the entry-level segment of the mainstream PC market. If WinChip 4 slips much, or misses its speed targets, it could meet the same fate as earlier WinChips.

IDT's saving grace may be that, unlike its larger competitors, it has less investment in its x86 business and lower overhead. Although AMD is losing money shipping 20 million processors per year at average prices that are more than twice IDT's, IDT believes that its x86 business could be profitable shipping only a few million units per year at an average price below $40. If IDT can deliver on this plan, it could be the supplier of choice at the very low end of the market. M