Mips and Chartered Form Unique Partnership

Mips Technologies and Chartered Semiconductor have formed a new partnership that allows customers to use Mips's latest CPU cores without negotiating a MIPS license or porting the soft cores to an IC process. Mips and Chartered say the unique arrangement will expand the market for embedded MIPS processors while saving customers the time and cost of porting cores to silicon.

Under the terms of the agreement, Chartered is a licensed foundry partner for the new MIPS32 4Kc and 4Kp Jade cores (see MPR 5/31/99, p. 18). Chartered will port the cores to its 0.25-micron process by 4Q99 and later to a 0.18-micron process in 1H00 and a copper 0.18-micron process (developed with Lucent) in 2H00. Customers who want to integrate the cores with standard-cell macros can deal directly with Chartered by signing a simplified MIPS license. In return, they'll get the timing models, abstract files, and test vectors needed to design around the MIPS core. Chartered will drop the core into the customer's design and manufacture the wafers. Customers pay predefined royalties to Mips based on volume.

Besides saving upfront licensing fees, porting costs, and development time—not to mention the risk of botching a silicon port—customers are also insulated from Mips's intellectual property. They can develop their own designs without fear of "contamination." As a spokesman for Chartered put it, "They're not any more contaminated than an Intel customer who buys a Pentium."

Mips gets to sell more cores and collect more royalties. Mips says it prefers a business model based on royalties, not license fees—a model that has certainly paid off for Mips in its video-game deal with Nintendo (see MPR 6/1/98, p. 10). Chartered wins by becoming a larger supplier of MIPS-based chips, especially for smaller companies that can't afford the costs associated with a regular MIPS license.

One disadvantage is that customers have less control over the configuration of the prehardened cores, which partly defeats the purpose of choosing a soft core in the first place. Mips says it will offer several variations with different-sized caches to cover the most likely applications.

Mips's partnership with Chartered looks like a flank attack on Arm, which has been licensing its cores more widely than Mips. The strategy will probably attract startup companies and others that want a quick-to-market, black-box solution without having to pay multimillion-dollar upfront licensing fees. —*T.R.H.*

Motorola Plugs PowerQuicc Gap

Nature abhors a vacuum, and Motorola abhors gaps in its embedded product line. For customers who need an under-$40 communications controller with Fast Ethernet but not USB or more than one multiprotocol serial interface, Motorola is sampling the new PowerQuicc MPC855T. It fills a price and features gap in the PowerQuicc line between the six-member MPC850 family and the eight-member MPC860 family (see MPR 3/30/98, p. 12).

The 855T has one 10/100-Mbit/s Ethernet port and one serial communications controller (SCC) that supports several interfaces and protocols: high-level data-link control (HDLC), multichannel HDLC, ATM segment and reassembly (SAR), Motorola's serial peripheral interface (SPI), inter-IC (I^2C), and others. It also has a 4K instruction cache and a 4K data cache, and it runs at 50, 66, or 80 MHz. Prices range from $25 at 50 MHz to $32 at 80 MHz in 10,000-unit quantities.

All those features distinguish the 855T from other 850-series controllers, which have one or two 10-Mbit/s Ethernet ports, one or two SCCs, smaller caches, and a maximum frequency of 66 MHz. Some 850-series chips also have USB, which is absent from the 855T. At the high end, Motorola's 860-series controllers have even larger caches than the 855T, in addition to Fast Ethernet and up to four SCCs. The PowerQuicc line is unique in that no other chips have the same combination of a CPU core with integrated peripherals and a network protocol engine.

Motorola will sample the 855T this month and begin production in September. The chip is pin compatible with the 860 family but has 3.3-V I/O instead of 5-V I/O. It's the first PowerQuicc to make the transition to a 0.32-micron three-layer-metal process. Other members of the line are manufactured in a 0.42-micron process but will move to 0.32 micron in 3Q99. Unlike the 855T, however, they will retain 5-V I/O for backward compatibility.

Motorola expects the 855T to find its way into such products as cable modems, ADSL modems, small-office routers, and switching hubs for LANs. With more than 500 design wins for the PowerQuicc line—and a customer list that includes Cabletron, Cisco, Fujitsu, Lucent, Marconi, Nortel, Motorola's own business units, and many others—Motorola wants to cover every possible base with PowerQuicc variants. —*T.R.H.*

LSI Logic and Lucent Grow New ARMs

Both LSI Logic and Lucent have licensed the new ARM9E core (see MPR 6/21/99, p. 11). LSI has added the ARM9E to its CoreWare library and is targeting the mass-storage, digital-cellular, and voice-over-IP telephony markets. Lucent, which helped develop the core, is working with hard-drive manufacturers to create a single chip that integrates the ARM9E with Lucent's industry-leading read channel, disk-controller circuitry, and memory.

Lucent, which also recently licensed the ARM10 core, plans to fabricate the ARM9E-based chips in its 0.25-micron and other future IC processes. Clock speeds are expected to exceed 200 MHz. The first samples and evaluation systems are scheduled for release this fall. —*K.Y.*