AUDIO/VIDEO

Software for high-definition television sets. An introduction to the software running in an HDTV set—the present reality and speculation about future evolution. The central issue for today is MPEG processing. Peter Dibble, Microware; *Embedded Systems Programming*, 6/99, p. 22, 10 pp.

BUSES

Fundamentals of Firewire. The IEEE 1394 protocol (or Firewire, which is Apple's trademarked term) is one of the emerging bus protocols that will be important components of the connected future. Here's how it works. John Canosa, *Embedded Systems Programming*, 6/99, p. 52, 13 pp.

Digital buses, analog problems. The information that goes into and comes out of a bus is digital, but what goes on between input and output is analog. Thus, digital-hardware designers must learn to live in an analog world. Dan Strassberg, *EDN*, 5/27/99, p. 73, 9 pp.

DEVELOPMENT TOOLS

Firmware development on a virtual target. Entire systems can now fit on a single chip. This lowers system costs, but at the expense of additional complications for the firmware designers. How can firmware be developed and debugged in the absence of a physical prototype? C. Larry Rogers, *Embedded Systems Programming*, 6/99, p. 38, 8 pp.

DSP

DSP board designers balance processing power and bandwidth. Compensating for the system hooks that DSP chips lack, board vendors are crafting architectures that get the most out of DSPs. Jeff Child, *Electronic Design*, 6/14/99, p. 83, 6 pp.

IC DESIGN

FPGA high-level design methodology comes into its own. Learn why an HDL-based design flow may be just the thing for you and how to make sure you choose the right tools. Dave Kresta and Tony Johnson, Model Technology; *Electronic Design*, 6/14/99, p. 57, 3 pp.

An integrated functional performance simulator. The fMW simulation tool will help designers accurately evaluate the effectiveness of new microprocessor mechanisms and validate their correctness. Candice Bechem et al., Carnegie Mellon University; *IEEE Micro*, 5/99, p. 26, 10 pp.

Environment for PowerPC microarchitecture exploration. Microprocessor designers confront numerous options when evaluating different design possibilities. The authors' environment lets them explore the design space to determine the best mix of features. Mayan Moudgill et al., IBM T. J. Watson Research Center; *IEEE Micro*, 5/99, p. 15, 11 pp.

Verifying the FM9801 microarchitecture. Designers use formal logic and a theorem prover to verify that a complex microarchitecture always executes its instruction set correctly. Warren Hunt, Jr., IBM and Jun Sawada, Univ. of Texas; *IEEE Micro*, 5/99, p. 47, 9 pp.

MISCELLANEOUS

A peek behind the scenes at EEMBC. Two years after the formation of EEMBC, the first certified results from its industry-standard benchmarks are available. These results will provide you with an objective means of comparing processors and change the way you select processors for your designs. Markus Levy, *EDN*, 5/27/99, p. 93, 4 pp.

PERIPHERAL CHIPS

XLR8R: working with accelerometers. The ADXL202 two-axis ±2-g accelerometer from Analog Devices is a micromachine that's making waves in the commercial market. More sensitive than earlier designs, it's well suited for novel applications like two-axis tilt sensing and inertial navigation. Tom Cantrell, *Circuit Cellar*, 6/99, p. 78, 6 pp.

PROCESSORS

UltraSparc-III: designing third-generation 64-bit performance. Every decision has at least one associated trade-off. System architects ultimately arrived at this 64-bit processor design after a challenging series of decisions and trade-offs. Tim Horel and Gary Lauterbach, Sun; *IEEE Micro*, 5/99, p. 73, 13 pp.

Vying for the lead in high-performance processors. Sun's UltraSparc-3 could have a window of opportunity in the competition among high-performance 64-bit processors. Gary Lauterbach, Sun; *Computer*, June 1999, p. 38, 4 pp.

Performance analysis and validations of the PicoJava processor. This development team used simulator checkpoints to speed RTL model simulation, a simple and effective method that accurately analyzes performance and validates design. Sudheendra Hangal and Mike O'Connor, Sun; *IEEE Micro*, 5/99, p. 66, 7 pp.

PROGRAMMABLE LOGIC

Lies, damn lies, and benchmarks: the race for the truth is on. This hands-on project takes a fresh look at quantifying programmable-logic device capacity, efficiency, and performance. Brian Dipert, *EDN*, 5/27/99, p. 54, 9 pp.

SYSTEM DESIGN

Busted barriers. Moore's Law is on a collision course with U.S. export-control laws, prompting a debate over how, or even whether, to try to contain Information-Age hardware by applying Cold War–era export-control policies. Tam Harbert, *Electronic Business*, 6/99, p. 34, 6 pp.

Programmable logic: what's it to ya? Programmable logic is blurring the line between hardware and software. This report helps to put it in focus for embedded systems software developers. Michael Barr, *Embedded Systems Programming*, 6/99, p. 75, 8 pp.