Fujitsu FR-V Architecture Bets On VLIW

Customizable Instruction Set Optimized for Embedded Applications

by Tom R. Halfhill

Fujitsu Microelectronics has announced a new embedded-processor architecture that's definitely buzzword compliant. It has very long instruction words (VLIW), multimedia instructions, digital-signal-processing (DSP) features, a customer-extensible instruction set, and configurable cores. And the cores are designed to be combined with macro libraries to build system-on-a-chip (SOC) parts for consumer electronics, automotive-navigation computers, and communication devices.

Although Fujitsu *(www.fujitsu.com/micro.html)* won't disclose the full details about the new FR-V architecture until Microprocessor Forum in October, the company has sketched out the basics. FR-V builds on Fujitsu's considerable experience with FR-series microcontrollers, SparcLite processors, and supercomputer compilers. The goal is to provide a highly configurable architecture that's efficient enough for small, battery-powered products (such as cell phones and digital cameras) yet powerful enough for compute-intensive applications (such as digital TV, 3D graphics, and speech recognition).

As Figure 1 shows, Fujitsu has defined an instruction set divided into five subsets: 32-bit integer instructions, 16-bit integer instructions (for applications requiring greater code density), IEEE-754 floating-point instructions, multimedia instructions, and DSP instructions. Using tools that Fujitsu will supply, customers can combine these subsets in different ways and create their own application-specific instructions.

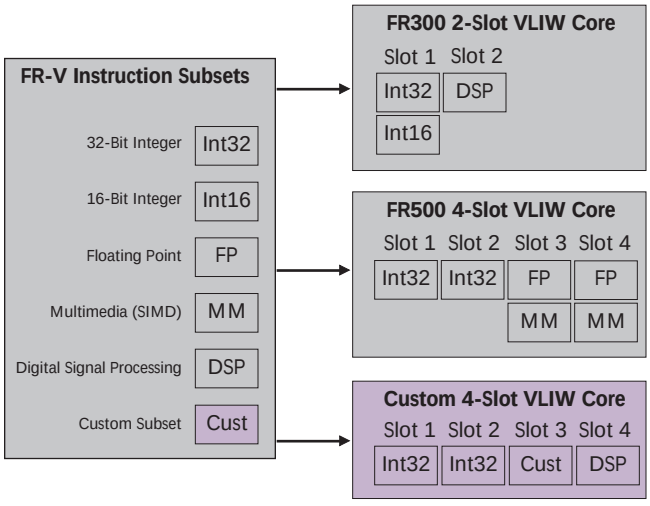

Figure 1. Cores may combine subsets of the FR-V instruction set in different ways. Customers can also define their own subsets. Some VLIW slots may contain different types of operations, such as floating-point or multimedia instructions.

The fixed-length instruction words can include one to four operations, with NOPs filling in any slots that the compiler can't schedule for parallel execution. Fujitsu claims its VLIW compiler will be good enough to allow most developers to use C or C++ instead of assembly language. Some third-party tool suppliers will support FR-V as well: Cygnus Solutions *(www.cygnus.com)* is porting GnuPro, and Gaio Technology *(www.gaio.com)* is porting its OpenPlus tools.

Two Cores Will Launch New Architecture

Fujitsu is working on two FR-V cores: the FR500, which has a four-way VLIW microarchitecture for higher-performance applications, and the FR300, which has a two-way VLIW design that's optimized for low power consumption—and in particular, for use in cell phones.

At its target frequency of 266 MHz, the FR500 will execute about 500 native MIPS, 1 GFLOPS, or nearly 4.3 billion operations per second when using single-instruction, multiple-data (SIMD) techniques. Fujitsu estimates the FR500 will consume about 1 W at a core voltage of 1.8 V in a 0.18-micron CMOS process. It's scheduled to be available in December. Fujitsu expects FR500-based chips to cost less than $25 in 10,000-unit quantities.

The FR300 will execute about 500 million SIMD operations per second and is expected to consume less than 25 mW, using a 1-V core in the same process. Samples won't be available until 4Q00. Fujitsu expects FR300-based chips to cost less than $12 in 10,000-unit quantities when they enter full production in 2001.

Fujitsu's roadmap isn't very aggressive in terms of clock frequencies. Not until after two process shrinks (to 0.13 and 0.10 micron) does Fujitsu expect the FR500 to reach 500 MHz. In contrast, Intel's second-generation StrongArm core is expected to hit 600 MHz in a 0.18-micron process while still consuming less than 500 mW.

Although Intel's IA-64 processors and some high-end DSPs are embracing various forms of VLIW, it's an unconventional architecture for embedded processors. Developers will have to rely more heavily on high-level language compilers than ever before.

If the compilers have trouble scheduling instructions for parallel execution and pad the instruction words with too many NOPs, the resulting code bloat will inflate memory requirements, system costs, and power consumption—all critical considerations for embedded systems. As Fujitsu discloses more details, it will be interesting to see how the FR-V architecture addresses those challenges. M