Teak Fills Gap Between Oak and Palm

DSP Group Improves Architecture With More Resources, Better Design

by Krishna Yarlagadda

To meet the growing needs of the ASIC vendors for more MIPS and ease of integration, leading DSP core vendor DSP Group released Teak—the follow-on to TeakLite. The Teak family is the third generation in the company's portfolio of licensable DSP cores and is supposed to fill the gap between the company's low-end Pine and Oak (see MPR 8/1/94, p. 1) and its high-end Palm. The Teak family maintains binary compatibility with the previous two generations (Pine and Oak).

TeakLite and Teak offer different performance levels. TeakLite is targeted at cost-sensitive applications, such as modems, cell phones, and VoIP (voice-over-IP) terminals. Teak is aimed at higher-performance applications, such as third-generation cellular phones, fast modems, and VoIP gateways. Both cores are 16-bit fixed-point DSPs. TeakLite executes the same instruction set as Oak, whereas Teak has additional instructions to utilize the added hardware.

Unlike Pine and Oak, Teak and TeakLite are fully synthesizable soft macros, making it easier for DSP Group and its licensees to port the design to different fabrication processes. National Semiconductor, Samsung Electronics, and Sony have already announced deals with DSP Group to license Teak.

Teak Adds Multiplier to Oak, TeakLite

As Figure 1 shows, Teak consists of four execution units: the CU (computation unit), BMU (bit-manipulation unit), DAAU (data address arithmetic unit), and PCU (production control unit). The computation and bit-manipulation unit consists of four 40-bit accumulators; two multipliers (16 × 16 → 32); a three-input, 40-bit split ALU; a 40-bit barrel shifter; hardware support for Viterbi; and exponent evaluation and normalization. The CU supports double-precision multiplies (all variations of signed and unsigned operations), and it is capable of performing dual multiply-accumulates (MACs) in a single cycle. Teak performs exponent evaluation in a single cycle and a full normalization operation in two cycles.

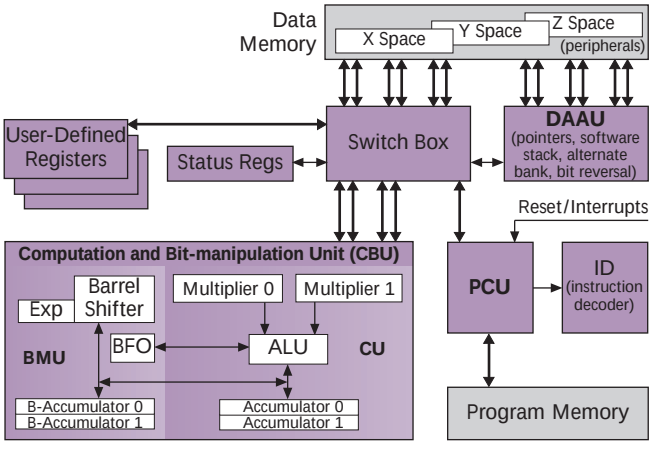

Figure 1. The Teak core adds a multiplier to improve performance over the Oak and TeakLite cores.

The DAAU consists of twelve 16-bit general-purpose pointer registers and two dedicated address arithmetic units for data memory (RAM/ROM). It supports indirect addressing, index-based addressing, and circular buffering. Teak supports a software stack and a zero-overhead looping mechanism with infinite nesting levels. Teak also has an option to add up to four 16-bit user-defined registers that are used for hardware accelerators and/or coprocessor support.

Improved Performance and Clock Frequency

Teak is expected to run at 140 MHz with a sustained MIPS rating of 180 Oak-equivalent MIPS in a 0.25-micron process and 110 MHz (140 MIPS) in a 0.35-micron process. As Table 1 shows, Teak offers a significant improvement in cycle count for some of the key DSP inner loops when compared with TeakLite. Teak is designed in a single-edge clocking system, which allows the use of full- or partial-scan testing methods.

The 0.25-micron Teak core measures just 1.7 mm^2 and is designed for operation below 1 volt, drawing only 0.25 mA/MHz in active mode. Teak supports emulation, debugging, and testing via a standard JTAG port. The complete Teak package includes hardware and software development tools and a TDKit (Teak development kit), which incorporates a development chip and board. M

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Algorithm	Oak DSP Core and TeakLite	Teak
Ntaps FIR (single sample)	N	N/2
Real Block FIR	NT	NT/2
Complex Block FIR	4N	2N
LMS Adaptive Filter	5N	2.5N
Biquad IIR	6	3
Vector Dot Product	T	T/2
Vector Maximum	T	T
256 Complex FFT Butterfly	14 w/rnd, 16 w/o	5
Viterbi Decoder	HW accelerator	3

Table 1. Teak offers a significant performance improvement over Oak and TeakLite on most DSP benchmarks. N is the number of filter taps. T is the number of points. (Source: DSP Group)