LX4280 Fills Lexra's Midrange

Lexra has announced a MIPS-compatible embedded processor core that it claims will be the fastest such 32-bit core on the market. The new LX4280 is expected to deliver 275 Dhrystone MIPS at a worst-case clock frequency of 200 MHz. At its maximum estimated frequency of 266 MHz, the LX4280 should deliver at least 350 MIPS.

That's up to 35% faster than Lexra's own LX4180 and about 70% faster than the maximum estimated performance of the new MIPS32 4Kc "Jade" core from Mips Technologies (see MPR 5/31/99, p. 18).

Performance comparisons are tricky, however, because Lexra is estimating the LX4280's frequency range in a 0.18-micron process, while Mips is expecting the 4Kc to run at 150–225 MHz in a 0.25-micron process. The race will be closer when the 4Kc is ported to a comparable geometry, although the single-issue Mips core will still be at a disadvantage because the LX4280 has dual-issue integer pipelines. Embedded-system designers who need greater code density will also appreciate Lexra's support for the condensed MIPS-16 instruction set—a feature that Mips omitted from the new Jade cores.

In terms of features as well as performance, the LX4280 is a significant addition to Lexra's lineup. It fits neatly between the LX4180, introduced in January (see MPR 1/25/99, p. 9), and the LX5280, announced at Embedded Processor Forum in May (see MPR 5/10/99, p. 5). While the LX4180 has a five-stage scalar pipeline and the LX5280 has a seven-stage superscalar pipeline, the new core splits the difference with a six-stage superscalar pipeline. Another important difference is that it lacks the Radiax DSP extensions introduced with the LX5280.

For those reasons, the new core can be viewed as a stretched version of the LX4180 or as a stripped-down LX5280. The hybrid pipeline is the most distinguishing feature. Unlike the LX4180, the LX4280 has an extra stage at the front of the pipe for accessing instruction memory, so cache timing is less critical and the core is easier to work with. Compared with the LX5280 pipeline, the new pipeline has one less stage for accessing data memory—a reasonable compromise, because omitting the Radiax instructions reduces the amount of data the core needs to handle.

Lexra plans to deliver the LX4280 as a synthesizable RTL model in 4Q99 and as a "SmoothCore"—Lexra's term for an optimized hard macro—in 1Q00. Lexra's foundry partners include IBM, TSMC, and UMC.

The LX4280 core is expected to occupy 3.8 mm^2 of die area (excluding primary caches) and consume 180 mW in a 0.18-micron process. Lexra estimates that the core will account for less than 5% of the die area on a typical system on a chip. Lexra, which doesn't have a MIPS license, is candid about fees: a single-project license costs $425,000, and an unlimited design license is $2.25 million. Maintenance and support adds 12% to those costs, and fixed-price royalties are $1.35 per chip. —*T.R.H.*

LSI Logic Buys ZSP

System-on-a-chip powerhouse LSI Logic has purchased DSP startup ZSP Corp. Though neither company will comment, it appears the transaction took place several weeks ago.

ZSP's unusual ZSP164xx processor architecture adapts elements of modern RISC CPU design, yielding a high-performance superscalar fixed-point DSP. The company first demonstrated the ZSP16401 running at 200 MHz in late 1998. Nearly a year later, the '401 remains the second-fastest fixed-point DSP, trailing only Texas Instruments' flagship TMS320C62xx DSP family.

ZSP aimed its initial devices at the growing market for telecom-infrastructure equipment, such as cellular-telephone base stations and voice-over-IP gateways. Competing head to head with market-share giants TI and Lucent, ZSP apparently was unable to gain a foothold in that market, despite its success at building initial silicon.

LSI Logic has long used DSP Group's Oak DSP core (see MPR 8/1/94, p. 1) in its DSP-oriented application-specific standard products (ASSPs), such as chips for GSM cellular phones. More recently, LSI licensed the innovative Carmel DSP core (see MPR 12/28/98, p. 18) from Infineon.

LSI's purchase of ZSP marks the first time the company has assumed ownership of a DSP architecture. Though LSI says an announcement about its DSP strategy is coming soon, at present it's unclear how the ZSP acquisition will affect LSI's plans for Carmel. It is also unclear whether the ZSP architecture will allow LSI to expand its reach beyond low-cost DSP-based devices and into higher-performance applications. —*Jeff Bier, BDTI*

Trimedia 1300 Arrives Late, Slow

Philips has begun sampling the TM-1300, the newest member of the TriMedia family of media processors. Though Philips promised the part would sample by the end of 1998 at speeds up to 180 MHz (see MPR 10/26/98, p. 33), it was late to arrive and is initially available at only 143 MHz.

Philips says it will sample a 166-MHz version of the TM-1300 in the third quarter, followed by the 180-MHz part in 1Q00. The 143- and 166-MHz parts will enter production in 4Q99. Philips hasn't announced a production schedule for the 180-MHz part.

The TM-1300 is manufactured in a 0.25-micron process and sells for as little as $35 in large quantities. That's about 40% less than its predecessor, the TM-1100. As it has with previous TriMedia products, Philips will sell the TM-1300 as a video processor for editing, conferencing, and security systems as well as for advanced set-top boxes. —*P.N.G.*