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Athlon Outruns Pentium III

With Future on the Line, AMD Rolls Out Athlon

by Keith Diefendorff

Repeating its 1997 feat with the K6, AMD has once again delivered the world's fastest x86 processor. Unlike the K6, however, which held that title for all of two weeks, AMD's new Athlon processor could hold it for a year or more.

In June, AMD began sampling the K7 at 500, 550, and 600 MHz, making good on the promise it made at last year's Microprocessor Forum. In July, the company announced the product name, Athlon (see MPR 7/12/99, p. 1), and this month it is officially launching the processor along with systems from top PC vendors, including Compaq and IBM.

As a last-minute surprise, AMD announced it will ship Athlon at 650 MHz, a move undoubtedly designed to one-up Intel's current top-end 600-MHz Pentium III (see MPR 8/2/99, p. 5). On top of this violation of Intel's birthright, AMD presented benchmarks that show Athlon to be significantly faster per clock cycle than Pentium III.

This situation may not change for Intel until it delivers its 0.18-micron Coppermine version of Pentium III in November. We expect this part to debut at 667 MHz and move rapidly to 733 and 800 MHz. But AMD could still hold the lead if it can coax the 0.25-micron Athlon to 700 MHz and quickly transmogrify it to 0.18 micron. The company hopes to ship production 0.18-micron parts this year from Fab 25 in Austin as well as 0.18-micron copper Athlons in 1Q00 from its new Fab 30 in Dresden. If it can achieve these goals, AMD should hold the performance title at least until Intel ships its seventh-generation Willamette in 2H00.

Sensing that performance alone may not be sufficient, AMD is pricing its new processor aggressively. At the low end, AMD will ask $249 for the 500-MHz Athlon, only 8% more than Intel gets for its Pentium III-450 and 45% less than the Pentium III-500. AMD will price the high-end Athlon-650 at $849, only 3% higher than Pentium III-600.

You Bet Your Company

With the K6 family, AMD had gained a 15% unit share of the PC-processor market by the end of 1998. Because K6 parts have trailed behind Intel parts in performance and frequency, however, AMD has been forced to price those parts below Intel's Celeron, sacrificing profits for sales. In a not completely successful effort to boost frequency, AMD's fabs pushed the K6's 0.25-micron CS44E process beyond the limits of manufacturability. Doing so hurt yields, raised costs, and, again, sacrificed profits.

To escape from between this rock and hard place, AMD is betting its future on a new processor, plotting a rapid transition away from the K6. To distance the new processor from the K6, which is indelibly etched into the market's collective mind as a Celeron-class processor, AMD chose the name Athlon rather than K7.

As Figure 1 shows, AMD will initially position Athlon in the performance-PC segment, trying to establish the brand as the performance leader. With its higher frequencies and measurably better performance, AMD hopes the market will accept the notion of paying Pentium III prices for Athlons.

Once Athlon is in 0.18 micron, AMD will drive it and its derivatives up into the server space and down into the Celeron space. By late 2001, AMD expects Athlon-family

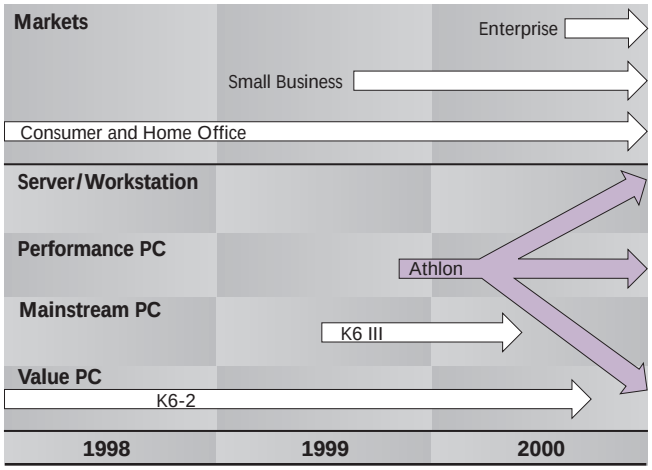

Figure 1. AMD's roadmap shows Athlon displacing K6 processors in all segments and entering the enterprise market in 2000.

processors will replace both the K6-2 and the K6 III. AMD has an aggressive goal of 30% unit market share by year-end 2000.

At lower frequency and voltage, the 0.18-micron Athlon may also reach into the high-power (over 14 W) mobile market, which AMD now serves with its K6-2P and K6 IIIP. It will probably take a shrink to 0.15 micron and 1.1 V, however, before AMD can use Athlon to reenter the sub-12-W mobile market it recently abandoned (see MPR 8/2/99, p. 5).

Three New Athlon Sub-brands on Tap

As Figure 2 shows, AMD divides the processor market in two dimensions: vertically into server/workstation, performance-PC, and value-PC segments as well as horizontally into consumer/small-business and enterprise markets. Initially, AMD is positioning Athlon in the performance-PC segment against Pentium III, where it has been unsuccessfully trying to peddle the K6 III.

Once rolling, AMD will extend Athlon horizontally into the enterprise market with Athlon Professional and upward into the server/workstation segment with Athlon Ultra, where it will compete head-on with Intel's Xeon. AMD will describe Ultra at Microprocessor Forum in October.

Athlon has obvious strengths for serving the enterprise markets. The design supports up to 8M of fast double-data-rate L2 cache, a fast system bus designed for speeds up to 400 MHz, and efficient MP support with its five-state MOESI cache-coherency protocol.

The barriers AMD must clear to enter the enterprise market, however, have more to do with the company's reputation and the industry's trust in it vis-à-vis Intel. The enterprise segments require more extensive testing, much higher reliability, and more system-management features than do the consumer segments. While Intel has earned its wings in these areas, AMD has never even had a processor that would fly. Athlon is suitable, but it will only enable AMD to begin knocking down the barriers. Simply overcoming the "nobody ever got fired for buying Intel" phenomenon in the enterprise market will be a challenge (see MPR 6/21/99, p. 20).

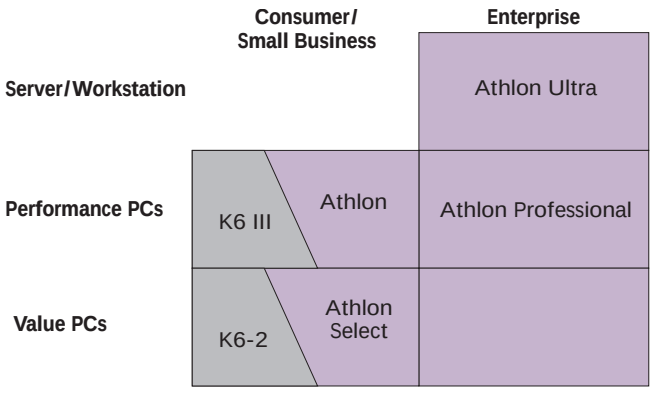

Figure 2. AMD will introduce three new Athlon sub-brands—Ultra, Professional, and Select—to differentiate its products in different market segments.

AMD is planning to enter the value-PC segment with the Athlon Select brand, eventually pushing out its own K6-2 processor. Competing effectively with Intel's Celeron in this segment, however, will require changes to Athlon. For one thing, Athlon will need an on-chip L2 cache to get away from module packaging and move to less expensive single-chip packaging. AMD must also keep its manufacturing costs under control, a challenge that will be made more difficult by the fact that the Athlon core is larger, albeit more powerful, than the Celeron core.

A major obstacle AMD will face in all segments is creating and sustaining a competitive chip-set infrastructure. Athlon's EV6 system-bus, while technically superior to Intel's P6 bus, precludes piggybacking on Intel's infrastructure. As a result, AMD must create its own infrastructure or wait for other vendors, such as Via, ALi, and SiS, to create chip sets. Although AMD's initial 750 "Irongate" chip set (see MPR 8/23/99, p. 12) is suitable for consumer, small business, and unbranded "white box" PCs, higher performance multiprocessor chip sets will be required for the enterprise markets, especially the server segment, and low-cost chip sets with integrated graphics will be needed for the value-PC segment.

Intel Not Screaming Uncle

Of course, AMD's plans are not sure things. Intel has tons of sand ready to shovel into AMD's gears. Although Intel may be fresh out of new microarchitectures until Willamette, it still has two weapons of mass destruction in its arsenal: IC process technology and manufacturing capability. AMD cannot match Intel on either of these fronts.

Despite Athlon's superior microarchitecture, Intel will use its extraordinarily fast 0.18-micron P858 process (see MPR 1/25/99, p. 22) to prevent AMD from getting too far ahead in frequency. AMD may eventually catch up as a result of its technology-development partnership with Motorola, but it's hard to see how AMD could get Athlon onto a new P858-class process and into high-volume production in a brand-new fab (Fab 30) before the middle of next year. Soon after that, Willamette will come to Intel's rescue.

Intel's manufacturing capability—by far the best in the world—will allow it to drive costs below AMD's. This advantage is magnified by the fact that Coppermine's core is smaller than Athlon's, even in the same IC process. With lower costs, Intel could try to price-cut AMD to death. Although Intel is in better condition to survive a price war, we believe it would be in neither company's best long-term interest to take this route (see MPR 8/2/99, p. 3). Therefore, we expect Intel to first try defending its turf with its process-speed advantage, launching a price war only as a last resort.

Athlon Touts Superior Microarchitecture

Although the P6 microarchitecture in Pentium III and the Athlon microarchitecture (see MPR 10/26/98, p. 1) are both three-issue out-of-order designs with long pipelines, Athlon's

is more aggressive in many ways. Athlon has fully general, symmetric instruction decoders, in contrast to P6's more restrictive asymmetric decoders; it also has much deeper instruction reordering hardware, more execution units (all fully pipelined), greater load/store reordering capability, higher L1-cache bandwidth, and a fully out-of-order 200-MHz system bus. All of these characteristics suggest that Athlon's microarchitecture will give it higher performance per cycle than Pentium III (see MPR 8/2/99, p. 1).

More Features Come to Light

Since AMD first described Athlon's microarchitecture at last year's Microprocessor Forum, it has made a few minor enhancements to the design and disclosed a few more details. At a Cahners MicroDesign Resources dinner meeting in June, Dirk Meyer, Athlon's chief architect, described additional details about the instruction control unit. The ICU controls instruction issue, register renaming, and out-of-order execution of integer instructions, as Figure 3 shows.

As Figure 4 shows, the ICU uses two distinct 24-entry register files—the future file and the architectural file—backed by a 72-entry reorder buffer. The future file (FF) holds the current state of the processor and is updated as instructions complete execution. Out-of-order results from the execution units are buffered in the reorder buffer (ROB) until they can be reassembled into program order and retired to the architectural file (AF).

On an exception, the processor can be quickly checkpointed back to a precise architectural state by a broadside copy of the AF to the FF. The broadside copy is facilitated by constructing the two files as a single unit with physically interleaved bits. AMD selected the future-file approach to avoid the time and complexity of the fully associative lookup required to locate the most recent version of each operand in a traditional reorder buffer.

Meyer also disclosed details about Athlon's branch predictor, which has been substantially improved over the simple PC-indexed local-history scheme of the original design. As Figure 5 shows, Athlon now employs a 4,096-entry branch-history table (BHT), with each entry containing a 2-bit prediction updated as a saturating up/down counter. The BHT is indexed using the Gshare technique (see MPR 11/17/97, p. 22) by an 8-bit global-history register hashed with four bits of the branch address.

Athlon's branch target address cache (BTAC) is integrated with the instruction cache. For each 16-byte fetch quantum, Athlon's I-cache maintains two branch target addresses, T_1 and T_2. Since the I-cache is 64K, the BTAC has 4,096 entries. Also, for each instruction byte pair in the I-cache, Athlon maintains a 2-bit selector that indicates whether the associated branch target is expected to be sequential, predicted by T_1 or T_2, or given by the return stack. Although Athlon's BTAC does not provide enough state to predict every branch target in a branch-rich code sequence, AMD claims that in practice the scheme provides nearly complete coverage.

Since the Forum, AMD also made a small but useful upgrade to Athlon's integer scheduler by increasing its capacity from 15 macro ops (30 ROPs) to 18 macro ops (36 ROPs). AMD says the increase boosted performance by 1–3% with no increase in silicon area or cycle time.

New Instructions Revealed

Perhaps the biggest surprise in AMD's recent disclosures is that Athlon will implement 19 new MMX/SSE and cache-control instructions plus 5 new DSP instructions. AMD labels these instructions collectively as "enhanced 3DNow." The 19 new instructions are identical to the "new media" instructions defined by Intel for SSE (see MPR 3/8/99, p. 7), plus SSE's nonbinding prefetch instructions.

The inclusion of these instructions will allow Athlon to compete on a level playing field with Pentium III on video encoding and decoding functions as well as on other integer

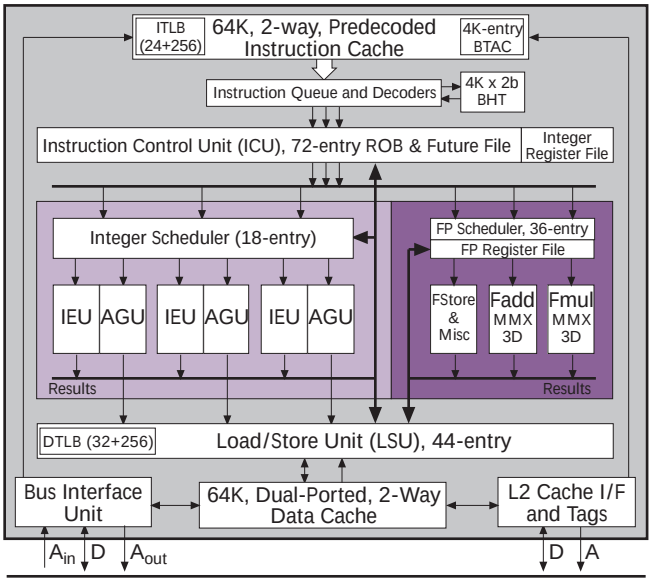

Figure 3. Athlon can decode up to three x86 instructions per cycle and issue up to nine ROPs per cycle out of order into its nine execution units. Up to 72 ROPs can be in flight at a time.

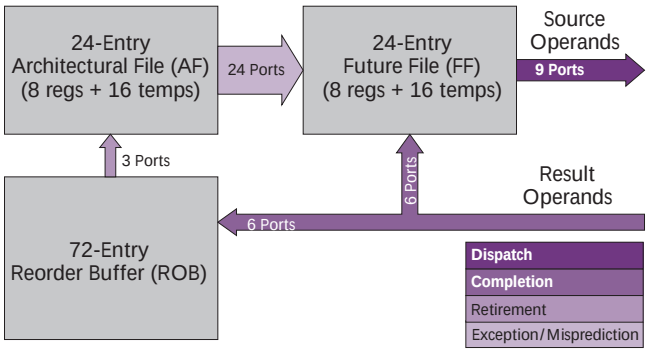

Figure 4. Athlon uses a future file to access source operands rather than the associative lookup used in classical reorder buffers.

multimedia applications. At the same time, they provide an additional measure of binary compatibility for those routines. These instructions do not, however, bring Athlon up to SSE's SIMD-FP standard.

While AMD is (presumably) working to integrate full SSE compatibility into Athlon, it will continue to tout 3DNow as providing equivalent SIMD-FP capability—which, in fact, it does, given Intel's half-wide implementation of SSE in Pentium III. In the meantime, AMD's installed base of 18 million 3DNow processors continues to hold developers' attention. AMD has even garnered mindshare from Microsoft, which has announced that 3DNow will be fully supported in its Visual C++ compiler as well as in Visual Studio.

AMD claims that its five new DSP instructions greatly improve Athlon's performance on applications such as soft modems, ADSL, complex math, and Dolby AC-3 and MP3 audio codecs. As Table 1 shows, these instructions, like other 3DNow instructions, operate on two-wide SIMD floating-point operands. With this innovation, AMD reaffirms its willingness to extend the x86 architecture beyond that defined by Intel. Given this inclination, we wouldn't be surprised to see AMD go beyond SSE when it finally does make this upgrade to Athlon.

Memory, the Proverbial Fly in the Ointment

Clearly, Athlon's core microarchitecture—at least when working into an infinite cache—should clean Pentium III's clock on integer and floating-point code. Athlon, however, will face the classical problem faced by all high-ILP cores: memory latency. Although Athlon's fancy reordering hardware provides some degree of latency tolerance, a simpler microarchitecture with a faster memory system might achieve similar performance.

On this, Intel is counting. Although rightly criticized for not having a new microarchitecture at this time, Intel has instead consciously chosen to spend its effort and its silicon on the memory system. Whereas Athlon splits its 22 million transistors evenly between logic and on-chip memory (two 64K L1s and tags for the off-chip L2), Coppermine puts only about 35% of its 23 million transistors in logic and the larger portion into memory (two 16K L1s and a 256K on-chip L2).

Since Intel has released no information about the speed or organization of Coppermine's L2, it isn't possible to determine whether Coppermine's or Athlon's approach will yield better overall performance. Athlon's approach does have the advantage of accommodating larger caches, which is a plus for the server market. But Athlon will not compete in the server market initially, and Coppermine's 256K L2 will be adequate for most PC applications. Considering that on-chip cache runs at full CPU clock speed, while external L2 is limited to half speed at best, Coppermine could have the advantage in memory system performance.

Athlon's choice of memory hierarchy puts it in a slight bind moving forward. As it migrates to 0.18 micron, Athlon's core frequency will rise substantially: 800 MHz, 1 GHz, maybe more. At these speeds, Athlon will no longer be able operate its external L2 at half speed; it will be forced down to ½.5 speed. Even though its half-increment dividers avert backing off all the way to ⅓ speed, Athlon's L2 will still be slower than Coppermine's full-speed on-chip L2, which scales right along with core frequency.

AMD presumably will create a derivative of Athlon with on-chip L2, but the change will be more costly than it will be for Coppermine. In 0.18 micron, both Coppermine and Athlon have about the same die size: slightly larger than 100 mm^2. Adding 256K of L2 cache to Athlon—which Coppermine already has—would boost its die size by 25% or so, making it more expensive to manufacture than Coppermine.

Furthermore, 256K of L2 would not be as effective on Athlon as on Coppermine. Since the ratio of L2 to L1 size would be only 2:1 on Athlon, compared with 8:1 on Coppermine, AMD would get less miss-rate reduction per L2-silicon dollar than Intel. Despite this fact, however, AMD says that large L1 caches are still the better tradeoff, and that Athlon would still benefit from a 256K on-chip L2, especially if it were highly associative. Implementing a larger on-chip L2, say 512K or 1M, would make the issue moot, but the die size would be prohibitively large for the PC market until Athlon is moved to the next-generation 0.15-micron IC process.

Another option would be for AMD to increase Athlon's L1 caches to 128K each, instead of adding an on-chip L2. But this move would almost certainly degrade frequency or add a

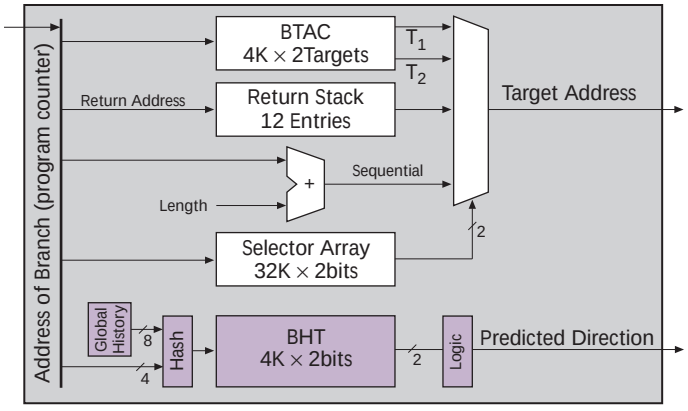

Figure 5. Athlon uses the Gshare variation of a two-level branch predictor to predict branch direction. Target addresses are predicted by a BTAC integrated into the instruction cache.

Mnemonic	Description	$A_1 \leftarrow$	$A_0 \leftarrow$
PF2IW	Packed FP to integer word convert	int16 B_1	int16 B_0
PI2FW	Packed integer word to FP convert	float B_1	float B_0
PFNACC	Packed FP negative accumulate	$B_0 - B_1$	$A_0 - A_1$
PFPNACC	Packed FP mixed +/– accumulate	$B_0 + B_1$	$A_0 - A_1$
PSWAPD	Packed swap doubleword	B_0	B_1

Table 1. Athlon adds five new 3DNow instructions to accelerate floating-point DSP code. The A_1 and A_0 columns show the results of an op $A_{1,0}$, $B_{1,0}$ instruction on the most-significant and least-significant halves of the 64-bit SIMD operands.

cycle of latency to every L1 access—probably not a good tradeoff. Decreasing the size of the L1 caches to make room for a 256K L2 is also a possibility. This approach, however, might require some pipeline redesign to avoid leaving L1 cycle time on the table.

None of these approaches seems ideal, so it appears that Intel may have selected the more scalable approach. Even in the short term, however, it is unclear how Athlon's more aggressive core will hold up against Coppermine's fast on-chip L2. The answer will remain a mystery until Intel delivers Coppermine in November. But for now, AMD can at least point to some compelling benchmark results that corroborate the superiority of Athlon's design over the current Pentium III, Katmai—both of which use off-chip L2s.

Benchmark Ground Rules

At its official launch on August 9th, AMD disclosed the results of its exhaustive benchmark testing of Athlon, which we have distilled here. Table 2 gives the system configurations AMD used for its tests.

The frequency at which to report benchmarks is a sticky issue. On the one hand, reporting results at the same frequency is appealing; it represents the relative performance of parts on a per-cycle basis. On the other hand, if the microarchitecture, design, or IC process of one chip gives it an inherent frequency advantage, that frequency is a legitimate component of the processor's ultimate performance and cannot be ignored when comparing it with other processors.

With respect to Pentium III and Athlon, it isn't clear which, if either, has a higher natural frequency. Since the 0.25-micron Pentium III is currently at 600 MHz and is not expected to go higher, and since Athlon is now at 650 MHz in 0.25 micron and Jerry Sanders has stated that it will be raised to 700 MHz in that process, it is tempting to credit Athlon with an inherent 8–17% frequency advantage. We are not quite ready to leap to this conclusion, however, because we have not yet been able to confirm that AMD isn't just pushing the L_{eff} of Athlon's gates to gain a frequency advantage for launch. AMD denies it.

Athlon Looking Good on Benchmarks

Figure 6 shows how Athlon compares to Pentium III on three industry standard benchmarks that focus on general-purpose integer code. SPECint_base95 is the integer-intensive component of SPEC's CPU95 test suite, commonly used in the scientific and technical community to measure workstation performance. On this test, the Athlon-550 scored 25.1, 6% higher than Pentium III Xeon-550. Athlon-650 scored 29.4.

Feature	Intel	AMD
Processor	Pentium III/Xeon (Katmai)	Athlon
Frequency	P III-600/Xeon-550	550, 600, 650 MHz
External L2	512K, half speed	512K, half speed
Chip Set	440BX/440GX	Irongate (AMD-750)
Bus Speed	100 MHz	200 MHz
Graphics	Diamond V770 (TNT2)	Diamond V770 (TNT2)
Hard Disk	WD41800, 18M EIDE	WD41800, 18M EIDE
Memory	128M PC100 SDRAM	128M PC100 SDRAM
Windows 98	First edition, DirectX 6.1A	First edition, DirectX 6.1A
Windows NT	Version 4.0, service pack 4	Version 4.0, service pack 4

Table 2. All benchmarks reported in this article were taken with these system configurations. (Source: AMD)

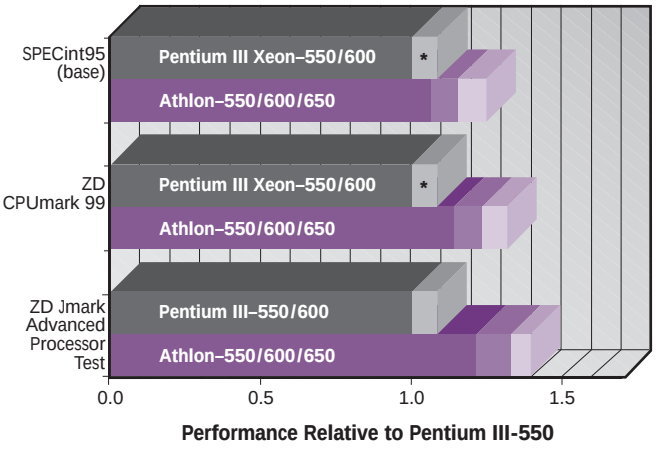

Figure 6. These benchmarks show how Athlon beats Pentium III on CPU-intensive integer code. (Source: AMD, except *MDR estimates)

CPUMark 99 is a component of the Ziff-Davis (ZD) WinBench 99 suite. This synthetic benchmark attempts to predict CPU performance in a PC environment by isolating it from the effects of graphics and disk performance. Figure 6 also shows the results from ZD's new JMark Advanced Processor Test, a test that evaluates the processor's performance running a Java virtual machine. On that test, Athlon-550 outperformed Pentium III-550 by 21%.

On floating-point tests, as Figure 7 shows, Athlon did even better. Athlon-650 delivered an impressive 22.4 on SPECfp_base95. Athlon-550 scored 20.6, outperforming Pentium III Xeon-550 by a whopping 36%. Less differential, only 7%, is seen on ZD's FPU WinMark—a component of the WinBench 99 v1.1 suite. Autodesk's AutoCAD 2000 program gives an 11% advantage to Athlon.

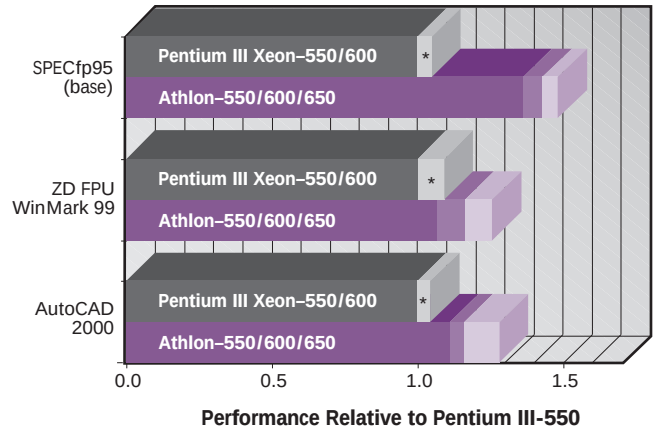

Figure 7. Athlon's three pipelined FPUs give it a big advantage over P III on floating point. (Source: AMD, except *MDR estimates)

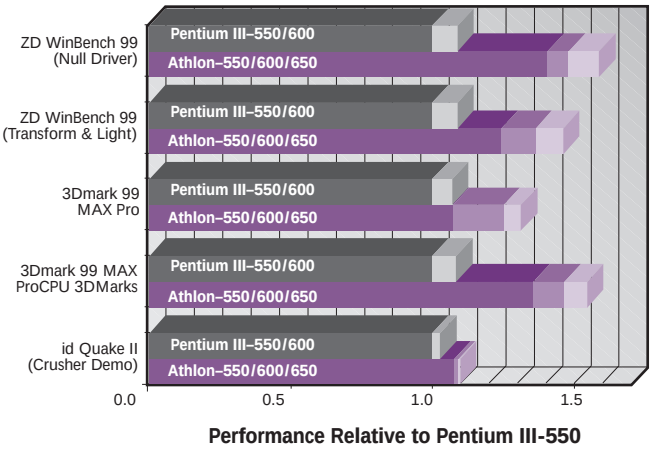

Figure 8. 3D benchmarks indicate Athlon's 3DNow implementation is a match for P III's SSE. (Source: AMD)

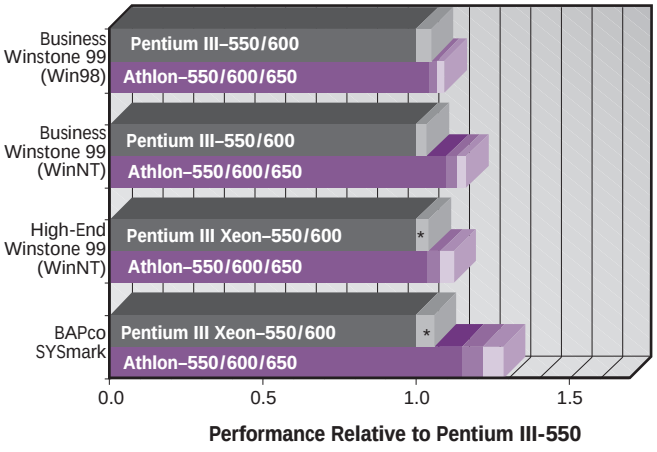

Figure 10. Even on application-level benchmarks Athlon's processing power shows through. (Source: AMD, except *MDR estimates)

Figure 8 shows the results of several 3D-graphics tests. These tests, like the previous ones, emphasize floating-point performance but, unlike the previous tests, exercise the SIMD-FP capabilities of Pentium III's SSE and Athlon's 3DNow. Shown are the results from ZD's 3D WinBench 99 v1.2 on Windows 98 using a null driver, as well as just the transform-and-lighting portion of the same benchmark. Both attempt to factor out the performance effects of the graphics rendering card.

Also shown in Figure 8 are the results from Futuremark's 3DMark 99 MAX Pro benchmark and its CPU 3DMark subset, as well as the Crusher Demo from Quake II, a popular performance benchmark used by the 3D-gaming industry. On the 3D tests, Athlon's per-clock advantage ranges from 7% to 41%, a result that substantiates AMD's claim that Athlon's 3DNow implementation is no less powerful than Katmai's implementation of SSE.

Athlon also takes the multimedia performance prize, outperforming Pentium III by 5–24% at the same frequency, as Figure 9 shows. The multimedia benchmarks include Microsoft's Windows Media Encoder compressing and encoding a 106-frame AVI file with the MPEG-4 codec; Adobe Photoshop 5.0 applying 42 common imaging functions and filters to four typical images; Dragon System's newest speech engine converting a WAV sound file to text; and LizardTech's MrSID Publisher for GeoSpatial compressing a 400M TIFF file by 20×. For all tests except Photoshop, the code was optimized for both SSE and 3DNow; the Photoshop test was optimized only for SSE, leaving Athlon with additional upside potential on this benchmark.

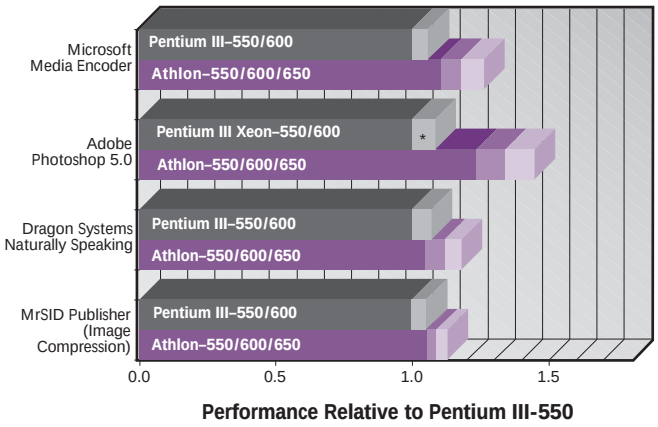

Figure 9. On multimedia-rich benchmarks, Athlon outperformed P III by 5% to 25%. (Source: AMD, except *MDR estimates)

As expected, the general-purpose application-level benchmarks show somewhat less benefit for the faster processor, a consequence of other system-performance factors diluting the results. Still, as Figure 10 shows, Athlon's performance lead was clear, ranging from about 4% to 15% on ZD's Business Winstone 99 (on both Windows 98 and NT), High-End Winstone 99 on NT, and the BAPco SYSmark suite on NT. These suites consist of scripts executing popular Windows-based applications, such as word processing, spreadsheets, project management, CAD, and presentation graphics programs.

Athlon the Clear Performance Leader

Unable to resist the urge to condense benchmark results into a single figure of merit, in Figure 11 we have provided the unweighted geometric means of the results from each benchmark category as well as the geometric mean of all the benchmarks. Although this method of summarizing results is unscientific and simplistic, in this case the results seem unambiguously clear. Athlon outperformed Pentium III in every category by a minimum of 8% and by an average of 15% at the same frequencies; by 11% and 20% if you include Athlon's current 50-MHz frequency advantage.

Admittedly, these benchmarks were selected and executed by AMD, a player with a vested interest in the outcome. But the benchmarks we've reported here are the same ones commonly cited by independent analysts. Since they represent a broad spectrum of application areas, and since they are consistent, it is unlikely that they distort the performance picture significantly. *PC Magazine* also tested Athlon and,

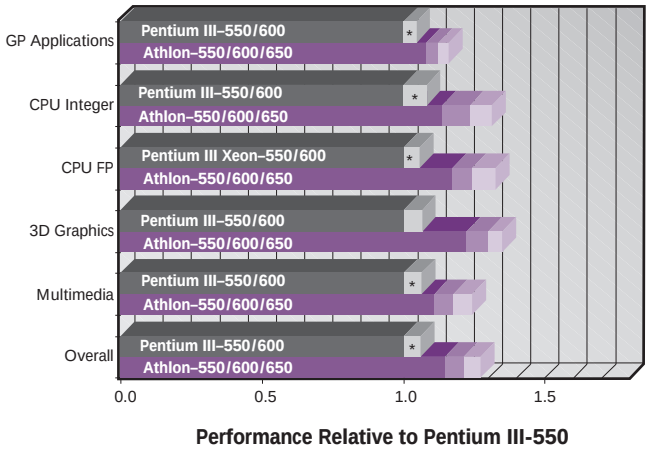

Figure 11. Athlon clearly outperforms Pentium III in every category. (Source: AMD, except *MDR estimates)

like AMD, found that Athlon outperformed Pentium III on every benchmark (except one minor game benchmark).

Athlon's performance has captured the interest of PC vendors. Although the complete list of Athlon adopters was not available at the time this issue went to press, all of the top-10 PC vendors, save for Dell, are already using AMD processors, and we expect they will also field Athlon systems. Compaq and IBM have both announced Athlon-based systems.

Compaq announced a $1,999 high-end consumer box, the Presario 5861, sporting a 600-MHz Athlon, 17" monitor, 13G disk, 128M DRAM, and Voodoo 3 graphics. IBM introduced two Aptiva S Series consumer systems: the top-of-the-line model 865 with a 650-MHz Athlon lists for $2,299 (DVD, 20G, 128M, and TNT2), while the 600-MHz model 860 lists for $1,999. IBM said it will soon announce four more E Series consumer systems with Athlons of various speeds. Neither company has yet announced a small-business system, but AMD expects they will.

Holding the performance lead over Intel, even by only a few percentage points, will be a powerful weapon for AMD. IBM marketing, for example, has already pointed out how its Athlon-based Aptiva outperforms Dell's Dimension on benchmarks. Once Compaq and other Athlon customers join this chorus, Dell could be forced to abandon its staunch Intel-only strategy. This would be a major victory for AMD, setting the stage for further market-share gains.

Looking Good So Far

Even allowing for a wide margin of error in these results, AMD has certainly accomplished its goal of beating Intel at its own game—performance. But while Athlon's performance lead seems sizable, the gap is likely to shrink from this point forward. Intel cannot afford to let this situation stand for long, and it will probably spare no expense to reverse it.

The first lever Intel will pull is Coppermine, supported by its new Camino chip set. With a full-speed on-chip L2, a 133-MHz system bus, and whatever other tricks Intel may be hiding up its sleeve, that processor will undoubtedly perform better than the current Pentium III on a per-cycle basis. Intel will also leverage its advanced P858 process to assure that AMD doesn't stay ahead in frequency, even though Athlon's microarchitecture might otherwise permit it. Coppermine's improvements, while unlikely to turn the performance table around, will definitely narrow the gap. With clever marketing, Intel could muddy the water enough to obscure Athlon's remaining performance lead.

Even though Athlon is a moral victory for AMD and an embarrassment for Intel that is sure to bruise its ego, the actual business threat Athlon poses to Intel must be placed in perspective. Athlon's volumes will initially be small, and AMD simply does not possess the manufacturing wherewithal to absorb a growth in demand large enough to seriously damage Intel's market share between now and Willamette. So while the economic upside potential for AMD is great, the situation for Intel is hardly apocalyptic.

Furthermore, while AMD may have won this performance battle, the war is far from over. Although Athlon gives AMD a strong product with which to compete, the company must still execute to capitalize on the opportunity. It must put Athlon into high-volume production, create a viable chip-set infrastructure, make a smooth transition to 0.18 micron, ramp in Fab 30, upgrade Athlon with on-chip L2 and SSE, and follow with a steady stream of compelling derivatives. And it must execute all of these tasks flawlessly, as there is no room for error when you're up against Intel. It is an immense problem for AMD that Atiq Raza, the driving force behind both the K6 and Athlon, will not be there to lead these coming battles (see MPR 8/2/99, p. 4).

Although it may yet crumble under the merciless attack Intel is sure to launch, at this point AMD deserves enormous credit for its Athlon achievement. With Athlon, AMD moves performance from a liability to an asset. For the first time, AMD will gain legitimate access to the performance-PC segment, where prices, and profits, are higher. The ability to deploy competitive products in this segment, as well as the low-end segments, will provide AMD with price protection, as Intel can no longer outflank it by slashing prices at the low end only to make up for it at the high end. Athlon is AMD's best opportunity for success in the company's long history. M

Price & Availability

AMD is currently shipping Athlon at speeds of 500, 550, 600, and 650 MHz. The 500-MHz parts list for $249, the 550-MHz parts for $449, the 600-MHz parts for $615, and the 650-MHz parts for $849, all in quantities of 1,000 units.

For more information about Athlon, check out AMD's Web page at *www.amd.com/products/cpg/athlon*.