AUDIO/VIDEO

SuperENC: MPEG-2 video encoder chip. Emerging multimedia applications, such as digital versatile disk and high-definition television, demand higher-quality video than ever before. In response, the SuperENC video encoder chip supports multiple profiles and levels. Mitsuo Ikeda, Nippon T&T; *IEEE Micro*, 7/99, p. 56, 10 pp.

The D30V/MPEG multimedia processor. This processor integrates a dual-issue RISC with minimal hardware support to implement a real-time MPEG-2 decoder. Its small chip area and easy programming are advantageous for multimedia applications. Hidehiro Takata et al., Mitsubishi Electric; *IEEE Micro*, 7/99, p. 38, 10 pp.

BUSES

CompactPCI: a market perspective. Even though CompactPCI has been around for a while, it hasn't gathered a lot of momentum. What will it take to enable this technology to find success? Jerry Krasner, *Embedded Systems Programming*, 7/99, p. 52, 4 pp.

DEVELOPMENT TOOLS

Hardware-software codesign of an image processing unit. A codesign tool suite helped handle the demands of hardware-software codesign by facilitating architectural exploration, partitioning, scheduling, and interface synthesis. Clarisse Adida, Aerospaciale Missiles, et al.; *ISD*, 7/99, p. 37, 5 pp.

Emerging trends in PLD tools. Process advances and new design methodologies push programmable logic tool vendors to extend tools to accommodate multiple processors, widely dispersed work groups, and Web support. Martin Won and Balaji Thirumalai, Altera; *ISD*, 8/99, p. 26, 4 pp.

DSP

DSP doings. Top suppliers TI, Lucent, Motorola, and Analog Devices are all making strategic alliances and acquisitions to position for the next wave of growth. Tom Cantrell, *Circuit Cellar*, 8/99, p. 76, 6 pp.

IC DESIGN

Design challenges of technology scaling. An analysis of microprocessor performance, transistor density, and power trends through successive technology generations helps identify potential limiters of scaling, performance, and integration. Shekhar Borkar, Intel; *IEEE Micro*, p. 23, 7 pp.

Deep-submicron microprocessor design issues. To fully exploit shrinking feature sizes and avoid being overwhelmed by complexity, microprocessor designers must keep up with technology trends, understand specific applications, and use advanced CAD tools. Michael Flynn et al., Stanford University; *IEEE Micro*, 7/99, p. 11, 10 pp.

Raptor II: using IP to make a better camera. A fully synthesizable core helps Sierra Imaging design an SOC for digital cameras with less time and effort. Nick Flaherty, *Silicon Strategies*, 7/99, p. 18, 4 pp.

Tell me again—what does the "S" in SOC stand for? Because sequential steps in designing SOCs often occur simultaneously or with many iterations, codesign can rapidly turn into chaos without a clear flow and the software to keep it all under control. Takashi Hasegawa, Fujitsu, and John McNally, Coware; *ISD*, 7/99, p. 15, 4 pp.

It's alive. After a three-year illness, semiconductor capital equipment makers and their customers are emerging from hard times. Howard Rudnitsky, *Electronic Business*, 7/99, p. 68, 4 pp.

System-on-chip design with virtual components. Design methodology and EDA tools are being severely stressed by SOC projects at the same time that narrowing time-to-market requirements demand more rapid and frequent introduction of new products. Thomas Anderson, Phoenix Technologies;*Circuit Cellar*, 8/99, p. 12, 7 pp.

MEMORY

Flash memory: past, present, and future. Many embedded developers think of flash as nothing more than a replacement for EPROM, but flash can also be used as a replacement for battery-backed RAM and bulk storage. Jack Ganssle, *Embedded Systems Programming*, 7/99, p. 59, 7 pp.

Flash memories do double duty. In the beginning, there was PROM, then EPROM, and then EEPROM—now there's flash-memory technology, which is an improvement over these technologies because it costs less and provides in-circuit programmability. Kenneth Ciszewski, *Circuit Cellar*, 8/99, p. 32, 5 pp.

PERIPHERAL CHIPS

Ring-based layer-3 switch drops port costs and improves efficiency. By lowering port costs tenfold, the first hardware-based routing engine eases the design of high-performance layer-3 switches. Dave Bursky, *Electronic Design*, 7/26/99, p. 41, 4 pp.

PROCESSORS

16-bit: the good, the bad, your options. Pressured from below and above, it would seem that the 16-bit market has little new to offer. A creative redefinition of "16-bit," however, opens new avenues. Rick Grehan, Metrowerks; *Embedded Systems Programming*, 8/99, p. 71, 6 pp.

PROGRAMMABLE LOGIC

Verilog simulation bridges the gap between PLDs and ASICs. Designers used a Verilog simulator and an ASIC design flow to create a PLD that would emulate an ASIC, enabling faster and more accurate verification and testing. Allen Vexler, System Design Group; *ISD*, 8/99, p. 19, 4 pp.

SYSTEM DESIGN

Micro-RISC architecture for the wireless market. Low-power, embedded, compiler-friendly processors provide increased functionality in highly integrated wireless handsets. David Gonzales, Motorola; *IEEE Micro*, 7/99, p. 30, 8 pp.