by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send e-mail to belgard@umunhum.stanford.edu *with comments or questions.*

5,862,370

Data processor system with instruction substitution filter for deimplementing instructions

Filed: September 27, 1995 Issued: January 19, 1999
Assignee: VLSI Claims: 10
Inventor: Kenneth Dockser

A data processing system including a microprocessor, memory, and an instruction-substitution filter. Configuration data indicating instruction types to be deimplemented is entered into the filter during the boot sequence. Once configured, the filter substitutes call instructions for the deimplemented instructions. When executed, the call instructions activate a substitution routine for the deimplemented instructions.

5,860,150

Instruction pre-fetching of a cache line within a processor

Filed: October 6, 1995 Issued: January 12, 1999
Assignee: IBM Claims: 24
Inventors: Kevin Chiarot et al.

An apparatus for fetching data from main memory into primary cache memory of a processor. Instruction fetch requests are generated by the processor and assigned a priority level. The highest priority level fetch request is serviced first. A prefetch request for cache line address N+1 is generated when a memory request for cache line N is generated, but is assigned a lower priority than an outstanding actual fetch request.

5,860,019

Data driven information processor having pipeline processing units connected in series including processing portions connected in parallel

Filed: July 10, 1996 Issued: January 12, 1999
Assignee: Sharp Claims: 21
Inventor: Manabu Yumoto

A dataflow processor has at least one pipeline stage with an input control processing portion to receive an input data packet from an immediately preceding pipeline stage. The input control portion outputs the packet to one output of multiple outputs, according to a prescribed method. Connected to each output is a data processing unit. Each of the data processing units operates on the data and produces an output data packet that is received by a common output control portion. The common output portion outputs the packet to an immediately succeeding pipeline stage.

5,860,018

Method for tracking pipeline resources in a superscalar processor

Filed: May 25, 1997 Issued: January 12, 1999
Assignee: Sun Claims: 8
Inventor: Ramesh Panwar

A method and apparatus for tracking pipeline resources of a processor by marking fetched instructions with instruction metadata. The instruction metadata indicates a number of pipeline resources required by each instruction. Using the cumulative instruction metadata, a count of a number of resources committed to issued instructions in the execution pipelines is maintained. This data is used to throttle instruction issue.

5,860,017

Processor and method for speculatively executing instructions from multiple instruction streams indicated by a branch instruction

Filed: June 26, 1996 Issued: January 12, 1999
Assignee: Intel Claims: 29
Inventors: Harshvardhan Sharangpani et al.

A microprocessor for efficient processing of conditional branch instructions. Branch prediction logic coupled to the fetch unit predicts the flow of a conditional branch. Stream-management logic directs speculative processing of instructions from both the first and second code sections prior to resolution of the condition, if resolution of the condition is unlikely to be predicted accurately.

5,859,999

System for restoring predicate registers via a mask having at least a single bit corresponding to a plurality of registers

Filed: October 3, 1996 Issued: January 12, 1999
Assignee: IDEA (Intel/HP) Claims: 21
Inventors: Dale Morris et al.

Method and apparatus for restoring a predicate register set. In response to an instruction specifying a predicate-register restoring operation, a mask is used to select the predicate registers that are to be restored. The mask of consists a set of bits, with each bit corresponding to a register in the predicate register set. Additionally, a single bit may be used to specify a predetermined set of registers to be restored.

OTHER ISSUED PATENTS

5,864,707 *Superscalar microprocessor configured to predict return addresses from a return stack storage*

5,864,697 *Microprocessor using combined actual and speculative branch history prediction*

5,864,690 *Apparatus and method for register specific fill-in of register generic micro instructions within an instruction queue*

5,859,997 *Method for performing multiply-substrate operations on packed data* M