IDT Unveils New 64600 Core

IDT is augmenting its line of MIPS-compatible processors with a third 64-bit core designed for high-performance embedded applications. The new RISCore 64600 has a dual-issue out-of-order microarchitecture with bilevel branch prediction, dual 64K primary caches, a vector floating-point unit, a vector integer unit, and special instructions for digital-signal processing (DSP).

The RC64600 was jointly developed with SandCraft, which contributed key technology for the multimedia and DSP functions. Not surprisingly, the RC64600 strongly resembles SandCraft's SR1-GX core (see MPR 7/12/99, p. 10), which is also a dual-issue out-of-order machine that executes MIPS instructions.

Like the SR1-GX, the RC64600 has a vector FP unit and an expanded ALU (in addition to the regular ALU) that executes DSP-type multiply-accumulate (MAC) instructions. The FP unit can perform vector operations on two 32-bit operands packed into a 64-bit FP register. There's also an integer-vector unit that can operate on four 16-bit values in a 64-bit register. In all, the RC64600 can dispatch six instructions per cycle (two ALUs, one FP vector, one integer vector, one branch, and one load/store), though it can fetch and retire only two instructions per cycle. As many as 32 instructions can be pending in reservation stations ahead of the function units for out-of-order dispatch.

The RC64600 is based on the MIPS-IV architecture, but it adds several enhancements. One is an extended register file that allows a two-level exception scheme. The new "fast exceptions" swap out eight general-purpose registers into the extended registers for faster exception handling. Another enhancement modifies the TLB so multitasking processes can share data more easily. Together, these improvements boost the performance of real-time processing, software emulation of hardware, and context switching.

IDT plans to sample the first RC64600-based processor in 1Q00. It will debut at 400–500 MHz, which should yield over 800 Dhrystone MIPS. IDT will manufacture the chips at its Oregon fab in a 0.18-micron IC process. The core runs at 1.8 V with 2.5-V I/O that tolerates 3.3-V inputs. Power consumption is about 6 W. Pricing will be announced later.

The RC64600 is a powerful addition to IDT's 64-bit line, which already includes the RC4000 and RC5000 cores and eight processors. SandCraft's multimedia extensions should widen the potential market to include consumer-oriented information appliances, such as digital set-top boxes. That would also be a smart strategy, because IDT's core business—communications—faces a new threat from Intel's IXP1200 (see MPR 9/13/99, p. 1). IDT and other CPU vendors will need high-performance cores like the RC64600 to meet the challenge of new architectures optimized for networking tasks. —*T.R.H.*

AMD Teaches Old Core New Tricks

AMD has announced the Elan SC520, the first in a new series of its x86-based processors for embedded applications. Although the SC520 is based on the same 5x86 (actually a 486) core as previous 4xx-series Elan chips, it adds an FPU, twice as much primary cache (16K), and a new debug unit.

The SC520 integrates PC/AT core-logic functions, plus a 33-MHz PCI 2.1 interface and a 66-MHz SDRAM controller that supports up to 256M of memory. There's also an 8-MHz full-duplex synchronous serial port (for SPI, MicroWire, or I^2C interfaces) and two 16550 UARTs. The AMDebug unit has a 256-entry trace cache and two interfaces (9-bit serial, 21-bit parallel).

AMD plans to offer the SC520 in two speed grades: 100 and 133 MHz. Performance is in the same range as a 100-MHz Pentium—about 90 Dhrystone 2.1 MIPS. AMD will sample the chips in 4Q99 and hopes to enter full production in 1Q00. Packaged in a 388-pin BGA, the SC520 will cost $33 at 100 MHz and $38 at 133 MHz in 10,000-unit quantities. Typical power consumption is 1.6 W at 133 MHz in a 0.25-micron IC process.

When AMD first introduced the Elan family in 1993 with a 386-based chip, potential customers shunned it, worried that it was a passing fancy. When AMD introduced a 486-based device, customers decided the Elan was here to stay and began buying both versions. It's not the fastest embedded processor, but it runs x86-based software, operating systems, and development tools, and it can squeeze the equivalent of a PC into a few square inches. That's enough to secure the Elan a place in the embedded market. —*T.R.H.*

New TriMedia Chips Come With New Roadmap

Philips has announced two new members of its TriMedia family of media processors. The NX-2600 and NX-2700 are the first in the new Nexperia line, though they lack what will be the most important element of future Nexperia chips—an integrated MIPS processor core to offload conventional processing tasks from the multimedia-optimized VLIW engine.

The two new chips were known as the TM-2SD and TM-2HD on Philips's previous TriMedia roadmaps (see MPR 10/26/98, p. 33). Both are aimed at the consumer HDTV market and can decode all of the ATSC standard formats. The NX-2600 is designed to display the decoded content on a standard-definition screen (up to 720 × 480 pixels), while the NX-2700 has a second port that supports high-definition monitors with up to 1,920 × 1,080-pixel resolution.

Philips says future Nexperia processors will integrate 32- or 64-bit MIPS cores with on-chip peripherals. Like today's TriMedia chips, these new devices will be sold into consumer-electronics applications. The MIPS-core option will make it easier to support Windows CE and other mainstream operating systems. —*P.N.G.* M