by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send e-mail to belgard@umunhum.stanford.edu *with comments or questions.*

5,870,599

Computer system employing streaming buffer for instruction preetching [sic]
Filed: October 17, 1997 Issued: February 9, 1999
Assignee: Intel Claims: 36
Inventors: Glenn Hinton et al.
Streaming-buffer renaming for memory accesses issued by a microprocessor to external memory allows up to N fetch accesses for M physical streaming-buffer locations, where N>M. When a fetch within the processor misses the instruction cache, the fetch address is placed in the streaming buffer. Data fetched from the memory is returned to the streaming buffer into one of the M physical buffer locations. The data within the streaming buffer is returned to the instruction cache of the processor only if it is to be used in the computer program being executed.

5,870,597

Method for speculative calculation of physical register addresses in an out of order processor
Filed: June 25, 1997 Issued: February 9, 1999
Assignee: Sun Claims: 11
Inventors: Ramesh Panwar et al.
A method and apparatus for speculatively converting logical addresses to physical addresses in a processor using register windows. The processor has a window pointer register and a speculative window pointer register. A controller identifies an instruction expected to modify the value in the window pointer register and, in response, modifies the speculative value. A mapper converts the instruction-specified logical addresses to physical addresses based on the speculative value contained in the speculative window pointer register.

5,870,578

Workload balancing in a microprocessor for reduced instruction dispatch stalling
Filed: December 9, 1997 Issued: February 9, 1999
Assignee: AMD Claims: 31
Inventors: Rupaka Mahalingaiah et al.
A microprocessor employs a set of symmetrical function units, each of which is coupled into an issue position. Instructions are fetched and aligned to the issue positions. During clock cycles in which fewer than the maximum number of instructions are concurrently selected for dispatch to the issue positions, the microprocessor distributes the selected instructions among the issue positions in order to substantially equalize the number of instructions sent to each issue position over a number of clock cycles.

5,870,575

Indirect unconditional branches in data processing system emulation mode
Filed: September 22, 1997 Issued: February 9, 1999
Assignee: IBM Claims: 10
Inventors: James Kahle et al.
A processor and method of operation with a native instruction set that emulates guest instructions. Guest instructions and semantic routines formed of native instructions are stored in memory. The semantic routine to emulate a first type of unconditional indirect guest branch instruction calculates a speculative return address, stores it in memory, and branches to the target address. The semantic routine for a second type of unconditional indirect guest branch instruction reads the speculative return address from memory, fetches guest instructions at the speculative return address, and thereafter calculates a correct return address.

5,867,725

Concurrent multitasking in a uniprocessor
Filed: March 21, 1996 Issued: February 2, 1999
Assignee: IBM Claims: 24
Inventors: Patrick Fung et al.
A superscalar uniprocessor that performs concurrent multitask processing is provided. The processor maintains a complete set of program states for each task executing concurrently, allowing independent control of the program flows. The processor has multiple execution units that can execute tasks simultaneously and a dispatch unit that sends a retrieved instruction and a task tag to one of the execution units.

5,867,400

Application specific processor and design method for same
Filed: May 19, 1997 Issued: February 2, 1999
Assignee: IBM Claims: 29
Inventors: Hussein El-Ghoroury et al.
An architecture and methods of design for an application-specific processor with a high-level instruction set. The processor is based on predefined function blocks that each correspond to a specific instruction. Each instructions contains a "time" operand that determines when the clocks to the corresponding function block are activated.

OTHER ISSUED PATENTS

5,867,680 *Microprocessor configured to simultaneously dispatch microcode and directly-decoded instructions*
5,870,598 *Method and apparatus for providing an optimized compare-and-branch instruction* M