by Rich Belgard, Contributing Editor

The following U.S. patents related to microprocessors were issued recently. Please send email to belgard@umunhum.stanford.edu *with comments or questions.*

5,890,008

Method for dynamically reconfiguring a processor
Filed: June 25, 1997 Issued: March 30, 1999
Inventors: Ramesh Panwar et al. Claims: 8
Assignee: Sun
A method and apparatus for dynamically reconfiguring a processor by placing the processor in a first configuration having a first number *(m)* of strands while the instructions comprise instructions from a number *(m)* of threads. The instructions in each of the *m* threads are executed on one of the *m* strands using execution resources, at least some of which are shared among the strands. When the instructions originate from a different number *(n)* of threads, the processor is placed in a second configuration having a second number *(n)* of strands. The instructions are executed in each of the *n* strands, which also use execution resources, at least some of which are shared among the *n* strands.

5,887,161

Issuing instructions in a processor supporting out-of-order execution
Filed: March 31, 1997 Issue: March 23, 1999
Inventors: Hoichi Cheong et al. Claims: 20
Assignee: IBM
The invention relates to a method for issuing instructions in a processor. In one version of the invention, the method includes the steps of dispatching the instruction and source information to a queue, determining validity of the source information, and issuing the instruction for execution in response to the source information validity.

5,881,277

Pipelined microprocessor with branch misprediction cache circuits, systems and methods
Filed: June 13, 1999 Issued: March 9, 1999
Inventors: James Bondi et al. Claims: 16
Assignee: Texas Instruments
A microprocessor with a multistage instruction pipeline. Branch-prediction logic predicts a target instruction when a conditional-branch instruction is detected. The processor fetches a sequential group of instructions from the predicted target into the instruction pipeline. If the actual target does not match the predicted target of the conditional branch, the microprocessor successively fetches instructions from a sequential group of instructions stored in a storage circuit to one of the intermediary stages of the pipeline.

5,881,265

Computer processor with distributed pipeline control that allows functional units to complete operations out of order while maintaining precise interrupts
Filed: June 5, 1995 Issue: March 9, 1999
Inventors: Harold McFarland et al. Claims: 17
Assignee: AMD
Methods and apparatus for in-order retirement of data store operations in a processor. The invention writes a destination address into a write queue. Subsequent to execution of the operation, the invention stores data, to be stored in memory at the destination address, into the queue entry. Upon receipt of a signal, data in an entry of the queue is written into the memory/cache subsystem at the associated destination memory address.

5,881,262

Method and apparatus for blocking execution of and storing load operations during their execution
Filed: September 12, 1997 Issue: March 9, 1999
Inventors: Jeffery Abramson et al. Claims: 45
Assignee: Intel
A method and apparatus for performing load operations in a computer system is disclosed. The execution of a load operation is halted when a dependency exists between the load operation and another memory operation currently pending in the system. When the dependency no longer exists, the invention redispatches the load operation so that it completes.

5,881,258

Hardware compatibility circuit for a new processor architecture
Filed: March 31, 1997 Issue: March 9, 1999
Inventor: Siamak Arya Claims: 21
Assignee: Sun
A processor with separate instruction and data caches that executes instructions according to a new instruction set architecture, efficiently executes old software code by a compatibility circuit to receive old software instructions from a secondary memory, groups these instructions according to the new instruction set architecture and provides these grouped instructions to the instruction cache of the processor. The old instruction set is a subset of the new instruction set.

OTHER ISSUED PATENTS

5,884,071 *Method and apparatus for decoding enhancement instructions using alias encodings*
5,881,280 *Method and system for selecting instructions for re-execution for in-line exception recovery in a speculative execution processor*
5,878,261 *Method for restructuring code to reduce procedure call overhead* M