QUICKTAKE: WILLAMETTE REVEALED

Intel Demonstrates Next-Generation Processor Running at 1.5GHz

By Kevin Krewell {2/28/00-03}

The first public demonstration of the Willamette processor at this year's Intel Developers Conference (IDF) stole the show from the much-touted IA-64 Itanium processor. This seventh-generation IA-32 processor, in silicon only for a month, was demonstrated at 1.5GHz, although it ran only a CPU-megahertz meter. At some unspecified lower frequency, the Willamette processor was also used to run a number of other demos, including Intel Senior VP Dr. Albert Yu's PowerPoint presentation. Intel said the processor has already successfully booted all major operating systems.

Willamette will be packaged in flip-chip PGA (FC PGA) and was designed for a socket of between 400 and 500 pins, which Intel referred to as Socket-W. The unnamed Willamette bus is a source-synchronous 64-bit 100MHz bus that is quad-pumped to an equivalent of 400MHz per bit, delivering a total of 3.2GB/s of bandwidth—three times the bandwidth of the fastest Pentium III bus. The bus was described by Intel fellow and Willamette lead architect Glenn Hinton as very deeply pipelined, similar to the P6 protocol.

The chip set for Willamette, code-named Tehama, will be a dual-RAC (RDRAM) design similar to the 840. A dual-RDRAM design is capable of supplying the full bandwidth requirements of the Willamette front-side bus (a 266MHz DDR SDRAM can supply only 2GB/s). To keep Willamette's bus overhead low, the cache line was expanded to 128 bytes with 64-byte sectors.

Willamette Will (Double) Pump You Up

A unique and unexpected aspect of Willamette's microarchitecture is its "double-pumped" ALUs. Claiming the effective performance of four ALUs, the two physical ALUs are each capable of executing an operation in every half-clock cycle. It also appears that the load and store units can accept data on half-clock cycles. Although the amount of logic required to implement a quad ALU structure is reduced, one wonders what additional complexity this double-pumping introduced. The integer ALUs must be optimized to run at twice the CPU speed, which, in the case of the 1.5GHz demo, means the ALUs run at an incredible 3GHz. One side effect of the tight ALU timing budget appears to be that shift instructions have longer additional latency than those in the Pentium III.

The Willamette microarchitecture features a much deeper pipeline than that of the P6 microarchitecture; one example showed double the number of pipeline stages, from 10 to 20. The downside of this superpipelining technique is a large penalty for mispredicted branches. To compensate, designers improved the branch-prediction logic in Willamette and added a 4K branch-target array. Although details were in short supply, Willamette apparently employs greater speculative execution, allowing 100 or more instructions to be in flight at the same time—up to 48 outstanding loads and 24 stores are supported in the pipeline.

To reduce decode time in the main pipeline, Willamette introduces an execution trace cache that stores the decoded µOPs. The cache stores sequences of µOPs, including taken branches, as sequential strings of µOPs, eliminating the instruction fetch and decode latencies when the sequences are reexecuted.

SSE, Part Deux

The anticipated improvements to SSE, called SSE 2, were introduced in Willamette, including support for (dual) double-precision SIMD floating-point operations. In addition, Intel extended the MMX instruction set to include 128-bit instructions using the SSE registers (XMM registers). One of the "killer" applications for this new instruction format will be encryption and decryption code for the secure sockets layer (SSL). Utilizing the SSE registers for integer SIMD operands eliminates the need to use the MMX registers, and thus the context-switch overhead imposed by the EMMS instruction, which should be welcomed by programmers. Additional cache-control instructions were added to improve cache efficiency.

Die size and pricing were not disclosed at IDF. Intel did say it plans to ship "hundreds or thousands" of Willamettes by the end of the year, ramping to "millions" next year. ◇