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ITANIUM MEETS 800MHZ GOAL

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At the recent ISSCC, Intel VP Gadi Singer disclosed that the first Itanium products will achieve clock speeds of 800MHz. Although the company had not previously discussed clock speeds, this figure meets the internal goal that we have been reporting for some time (see *MPR 10/26/98-03*, "Intel Outlines High-End Roadmap"). This speed gives Itanium a shot at industry-leading performance.

Intel continues to be coy about the chip's actual performance, but Singer says its EPIC architecture will deliver better IPC (instructions per cycle) than competing designs that may reach faster clock speeds. In particular, he expects Itanium will deliver better native performance than the other chip Intel described at ISSCC, a 1GHz Pentium III. We continue to project scores of 50 SPECint95 (base) and 80 SPECfp95 (base), which would be consistent with Singer's statement.

Faster versions of Itanium may appear. Singer claims the clock speed has "lots of headroom," in part due to the use of opportunistic time-borrowing (OTB) domino circuits in critical pipeline stages. The OTB design allows time borrowing across clock phases, minimizing the impact of clock skew and reducing dead time between stages. We would not be surprised to see the 0.18-micron Itanium hit 866MHz or even 933MHz in 1H01.

Singer did not disclose the size of the on-chip caches but said that the Itanium module will contain up to 4M of external level-three cache that is four-way set-associative. This cache will be implemented with custom 1M cache chips similar to the ones Intel fabricates for its Pentium III Xeon processors. It will operate at the full speed of the CPU, delivering 12.8GB/s across a 128-bit bus (see *MPR 10/6/99-01*, "Merced Shows Innovative Design").

The system (front-side) bus peaks at 2.1GB/s by operating at 266 million transfers per second. We believe this is a 133MHz bus that transfers data on both clock edges. Other than the use of both clock edges, the Itanium bus appears to be much like the current P6 bus. It is 64 bits wide, supports out-of-order transactions, and uses GTL+ logic levels. The bus connects up to four processors without glue logic. Although this bandwidth is twice what current Xeon servers achieve, it is likely to trail the bandwidth of Alpha, UltraSparc-3, Athlon, and Intel's own Foster.

Still, Intel expects Itanium to deliver leadership OLTP performance in four-way servers, and we concur. Any deficiencies created by the bandwidth shortfall are likely to be overcome by the processor's excellent integer performance. The good news on clock speed indicates Itanium will be a formidable competitor in 2H00.